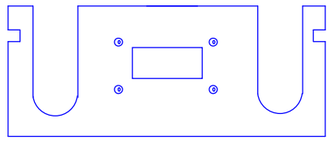
MODEL NAME : ***Centenario (DDP31)***

PCB NO : ***LA-G172P***

BOM P/N :

ZZZ1 LA-G172P_MB



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Schematic Document

(CENTENARIO ICE Lake U)

2019-05-29

Rev: 1.0 (A00)

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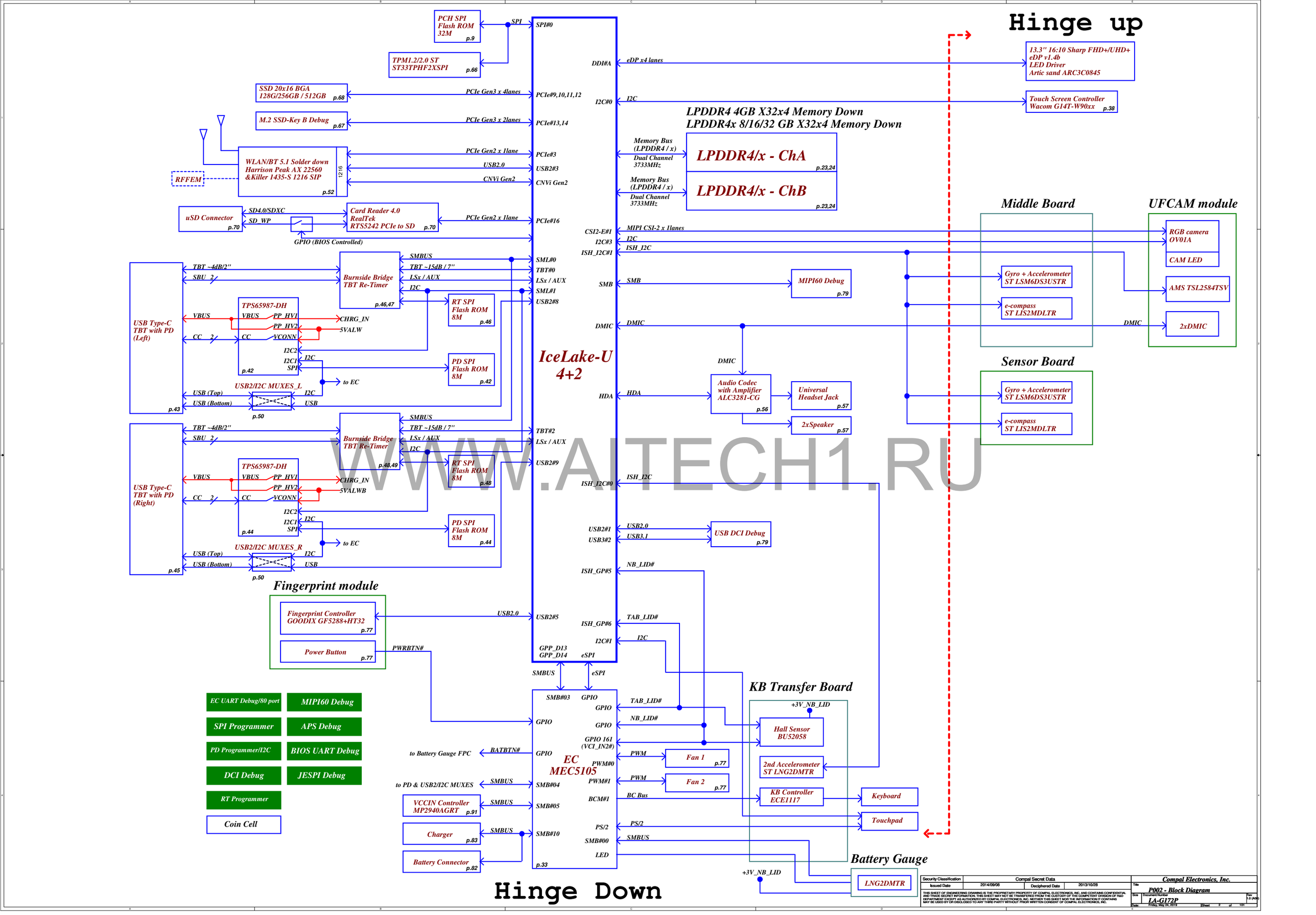
Title: ***P001 - Cover***

Size | Document Number: ***LA-G172P*** | Rev: 1.0 (A00)

Date: Wednesday, May 29, 2019 | Sheet 1 of 101


Hinge up
PCH SPI Flash ROM 32M p.9
SPI
SPI#0
TPM1.2/2.0 ST ST33TPHF2XSPI p.66
SSD 20x16 BGA 128G/256GB / 512GB p.68
PCIe Gen3 x 4lanes
PCIe#9,10,11,12
M.2 SSD-Key B Debug p.67
PCIe Gen3 x 2lanes
PCIe#13,14
RFFEM
WLAN/BT 5.1 Solder down Harrison Peak AX 22560 &Killer 1435-S 1216 SIP p.52
1216
PCIe Gen2 x 1lane
PCIe#3
USB2.0
USB2#3
CNVi Gen2
CNVi Gen2
uSD Connector p.70
SD4.0/SDXC
SD_WP
Card Reader 4.0 RealTek RTS5242 PCIe to SD p.70
PCIe Gen2 x 1lane
PCIe#16
GPIO (BIOS Controlled)
TBT ~4dB/2"
SBU 2
Burnside Bridge TBT Re-Timer p.46,47
SMBUS
TBT ~15dB / 7"
LSx / AUX
I2C
SML#0
TBT#0
LSx / AUX
SML#1
USB2#8
USB Type-C TBT with PD (Left) p.43
VBUS
CC 2
TPS65987-DH p.42
PP_HV1
PP_HV2
VCONN
CHRG_IN
5VALW
I2C2
I2C1
SPI
RT SPI Flash ROM 8M p.46
PD SPI Flash ROM 8M p.42
to EC
USB2/I2C MUXES_L p.50
USB (Top)
USB (Bottom)
USB
TBT ~4dB/2"
SBU 2
Burnside Bridge TBT Re-Timer p.48,49
SMBUS
TBT ~15dB / 7"
LSx / AUX
I2C
TBT#2
LSx / AUX
USB2#9
USB Type-C TBT with PD (Right) p.45
VBUS
CC 2
TPS65987-DH p.44
PP_HV1
PP_HV2
VCONN
CHRG_IN
5VALWB
I2C2
I2C1
SPI
RT SPI Flash ROM 8M p.48
PD SPI Flash ROM 8M p.44
to EC
USB2/I2C MUXES_R p.50
USB (Top)
USB (Bottom)
I2C
USB
IceLake-U 4+2
DDI#A
eDP x4 lanes
13.3" 16:10 Sharp FHD+/UHD+ eDP v1.4b LED Driver Artic sand ARC3C0845
I2C#0
I2C
Touch Screen Controller Wacom G14T-W90xx p.38
LPDDR4 4GB X32x4 Memory Down
LPDDR4x 8/16/32 GB X32x4 Memory Down
Memory Bus (LPDDR4 / x)
Dual Channel 3733MHz
LPDDR4/x - ChA p.23,24
LPDDR4/x - ChB p.23,24
Middle Board
UFCAM module
CSI2-E#1
MIPI CSI-2 x 1lanes
I2C#3
I2C
ISH_I2C#1
ISH_I2C
RGB camera OV01A
CAM LED
AMS TSL2584TSV
2xDMIC
DMIC
SMB
SMB
MIPI60 Debug p.79
Gyro + Accelerometer ST LSM6DS3USTR
e-compass ST LIS2MDLTR
Sensor Board
Gyro + Accelerometer ST LSM6DS3USTR
e-compass ST LIS2MDLTR
DMIC
DMIC
Audio Codec with Amplifier ALC3281-CG p.56
HDA
HDA
Universal Headset Jack p.57
2xSpeaker p.57
ISH_I2C#0
ISH_I2C
USB2#1
USB3#2
USB2.0
USB3.1
USB DCI Debug p.79
ISH_GP#5
NB_LID#
Fingerprint module
Fingerprint Controller GOODIX GF5288+HT32 p.77
USB2.0
USB2#5
ISH_GP#6
TAB_LID#
I2C#1
I2C
Power Button p.77
PWRBTN#
GPP_D13
GPP_D14
eSPI
SMBUS
eSPI
KB Transfer Board
+3V_NB_LID
Hall Sensor BU52058
2nd Accelerometer ST LNG2DMTR
KB Controller ECE1117
Keyboard
Touchpad
SMB#03
GPIO
TAB_LID#
GPIO
GPIO
NB_LID#
GPIO 161 (VCI_IN2#)
to Battery Gauge FPC
BATBTN#
GPIO
EC MEC5105
PWM
Fan 1 p.77
PWM#0
PWM
Fan 2 p.77
PWM#1
to PD & USB2/I2C MUXES
SMBUS
SMB#04
BC Bus
BCM#1
VCCIN Controller MP2940AGRT p.91
SMBUS
SMB#05
PS/2
PS/2
Charger p.83
SMBUS
SMB#10
SMB#00
SMBUS
Battery Connector p.82
LED
p.33
Battery Gauge
+3V_NB_LID
LNG2DMTR
EC UART Debug/80 port
MIPI60 Debug
SPI Programmer
APS Debug
PD Programmer/I2C
BIOS UART Debug
DCI Debug
JESPI Debug
RT Programmer
Coin Cell
Hinge Down
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Compal Electronics, Inc.
Title
P002 - Block Diagram
Size
Document Number
LA-G172P
Rev
3.0 (A00)
Date: Friday, May 04, 2018
Sheet 2 of 101

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	PCB Revision
0	240K +/- 5%	4700p	M00	0.1
1	130K +/- 5%	4700p	X00	0.2
2	62K +/- 5%	4700p	X01	0.3
3	33K +/- 5%	4700p	X02	0.4
4	8.2K +/- 5%	4700p	X03	0.5
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	1K +/- 5%	4700p		

SMBUS Control Table

	SOURCE	PCH	BATT Connector	Charger	VCCIN Controller	PD Controller	MIPI60	USB/I2C MUX	BurnSide Bridge	Accel+Gyro
PCH_SML0CLK PCH_SML0DATA	PCH								V	
PCH_SML1CLK PCH_SML1DATA	PCH					V			V	
SMBCLK SMBDATA	PCH						V			
EC_SMB03_CLK EC_SMB03_DAT	MEC5105	V								
EC_SMB04_CLK EC_SMB04_DAT	MEC5105					V		V		
EC_SMB05_CLK EC_SMB05_DAT	MEC5105				V					
EC_SMB10_CLK EC_SMB10_DAT	MEC5105		V	V						
EC_SMB00_CLK EC_SMB00_DAT	MEC5105									V

PCIE/USB3.1

Flexible I/O	Interface	DESTINATION
0	PCI-E#1 / USB 3.1#1	None
1	PCI-E#2 / USB 3.1#2	USB DCI Debug
2	PCI-E#3 / USB 3.1#3	WLAN PCIe Gen2(Reserve)
3	PCI-E#4 / USB 3.1#4	None
4	PCI-E#5 / USB 3.1#5	None
5	PCI-E#6 / USB 3.1#6	None
6	PCI-E#7	None
7	PCI-E#8	None
8	PCI-E#9	BGA SSD PCIe x4 GEN3
9	PCI-E#10	
10	PCI-E#11 / SATA#0	
11	PCI-E#12 / SATA#1a	
12	PCI-E#13	M.2 SSD Debug(Reserve)
13	PCI-E#14	
14	PCI-E#15 / SATA#1b	None
15	PCI-E#16 / SATA#2	Card Reader PCIE GEN2

USB 2.0

USB 2.0 PORT#	DESTINATION
1	USB DCI Debug
2	None
3	BT(Reserve)
4	None
5	FPR
6	None
7	None
8	Type-C_L
9	Type-C_R
10	None

CLK

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	WLAN(Reserve)
	CLKOUT_PCIE1	M.2 SSD(Reserve)
	CLKOUT_PCIE2	SSD
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	None
	FLEX CLOCKS	DESTINATION
	ESPI_CLK	EC eSPI

Thunderbolt

	TBT PORT#	DESTINATION
TBT	0	USB Type-C_L
	1	None
	2	USB Type-C_R
	3	None

CSI2

CSI2 PORT#	DESTINATION
C/D	None
E	UF
F	None
G/H	None

Displayport

	DDI PORT#	DESTINATION
DDI	A	4 Lane eDP
	B	None

Symbol Note :

@ : means de-pop

: means Digital Ground

: means Analog Ground

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Issued Date	2014/09/08	Deciphered Date	2013/10/28

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Title: P003 - Notes List

Size: | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 3 of 101

Centenario POWER BLOCK DIAGRAM

Power Rail

Audio Power Rail

2S2P Battery
51W

Type-C Port-L

Type-C Port-R

PD1
Controller
TPS65987DH

EC
MEC5105

PD2
Controller
TPS65987DH

Buck-boost
Charger
ISL9538B
(NVDC)
Page:83

B+

B+

B+

B+

PCH_PRIM_EN

+1.8VPRIM
TDC 2.56A
Peak Current 3.65A
(NB691)
Page:88

UC22
AOZ1334DI-01
CPU_C10_GATE#
+VCC1P8A

UC25
AOZ1336DI
AUD_PWR_EN
+1.8VS_AUDIO

UC24
AOZ1336DI
RUN_ON_P
+1.8VS

UC23
AOZ1334DI-01
SUS_ON_P
+1.8V_MEM

ALWON_3VALW

+3.3VALW
TDC: 5.1A
Peak Current 7.22A
(NB502)
Page:84

U7
SY6288
ENVDD
+LCDVDD

U31
AOZ1331DI
VCCDSW_EN_GPIO
+3V_PRIM
VCCDSW_EN_GPIO
+3VALW_DSW

U34
AOZ1331DI
WLAN_PWR_EN
+3VS_WLAN
TS_EN_R
+3VS_TS

UC30
AOZ1336DI
RUN_ON_P
+3VS

U51
AOZ1336DI
AUD_PWR_EN
+3VS_AUDIO

U733
AOZ1336DI
SSD_PWR1_EN
+3.3VDX_SSD

UC31
SY6288
SD_PWR_EN
+3VS_CR

UT1
AOZ1336DI
3.3V_TBT_L_EN
+3.3V_TBT_L

UT2
AOZ1336DI
3.3V_TBT_R_EN
+3.3V_TBT_R

Transfer Board

UKBC26
AOZ1336DI
TP_EN
+TRN_3VS_TP

IMVP_VR_ON_EN

VCCIN
TDC 36A
Peak Current 62A
(MP2940A)
Page:91,92,93

+VCC1.05_OUT_FET

UC13
AOZ1334DI-01
VCCST_EN
+VCCST_CPU

+VCC1.05_OUT_FET

UC12
AOZ1334DI-01
VCCSTG_EN
+VCCSTG_CPU

1.8V_PRIM_PG

VCCIN_AUX
TDC 10A
Peak Current 26A
(MP2941)
Page:89,90

+1.1V_MEM

UC27
AOZ1334DI-01
VCC_SFR_OC_EN
+VCC_SFR_OC

0.6V_VDDQ_EN_P

+0.6V_VDDQ (LPDDR4X only)
TDC 1.25A
Peak Current 1.79A
(NB691)
Page:87

1.1V_MEM_EN

+1.1V_MEM
TDC 4A
Peak Current 5.7A
(RT6243B)
Page:86

SSD_PWR3_EN_P

+SSD_PWR3
TDC 1.4A
Peak Current 2A
(NB693)
Page:95

U735
AOZ1336D
SSD_PWR3_EN
+SSD_PWR_3

SSD_PWR2_EN_P

+SSD_PWR2
TDC 1.4A
Peak Current 2A
(NB691)
Page:94

U734
AOZ1336D
SSD_PWR2_EN
+1.8V_1.2V_SSD

Q15
SI3457BDV
EN_INVPWR
+INV_PWR_SRC

ALWON_5VALW

+5VALW
TDC 5A
Peak Current 7.2A
(NB502)
Page:85

U36
AOZ1336DI
AUD_PWR_EN
+5VS_AUDIO

UPD1
TPS65987DH
+5VALWB_L_TBT

UC28
AOZ1336DI
RUN_ON_P
+5VS

U55
SY6288
3.3V_CAM_EN
+CAM_PWR

Middle Board

UMID1
RT9078N
+MID_CAM_PWR
+MID_UF_AVDD_2.8V

UMID2
RT9078N
+MID_CAM_PWR
+MID_UF_DVDD_1.2V

UMID3
RT9078N
+MID_CAM_PWR
+MID_UF_VDD_1.8V

ALWON_5VALWB

+5VALWB
TDC 3.5A
Peak Current 5A
(NB502)
Page:85

U60
AOZ1336DI
RUN_ON_P
+5VBS

UPD2
TPS65987DH
+5VALWB_R_TBT

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Date: Friday, May 24, 2019	Sheet 4 of 101		

Power On Sequence

[AC in]

ITEM	Measure Point			Time
Ta	TBT_VBUS	To	+3V_LDO	
Tb	+3V_LDO	To	+CHG_VIN_20V	
Tc	+CHG_VIN_20V	To	B+	
Td	B+	To	ACAV_IN	
Te	ACAV_IN	To	ALWON	
Tf	ALWON	To	+3VALW	
Tg	ALWON	To	+5VALW (+5VALWB)	
Th	+3VALW	To	ALW_PWRGD_3V_5V	

[Battery only, AC absent]

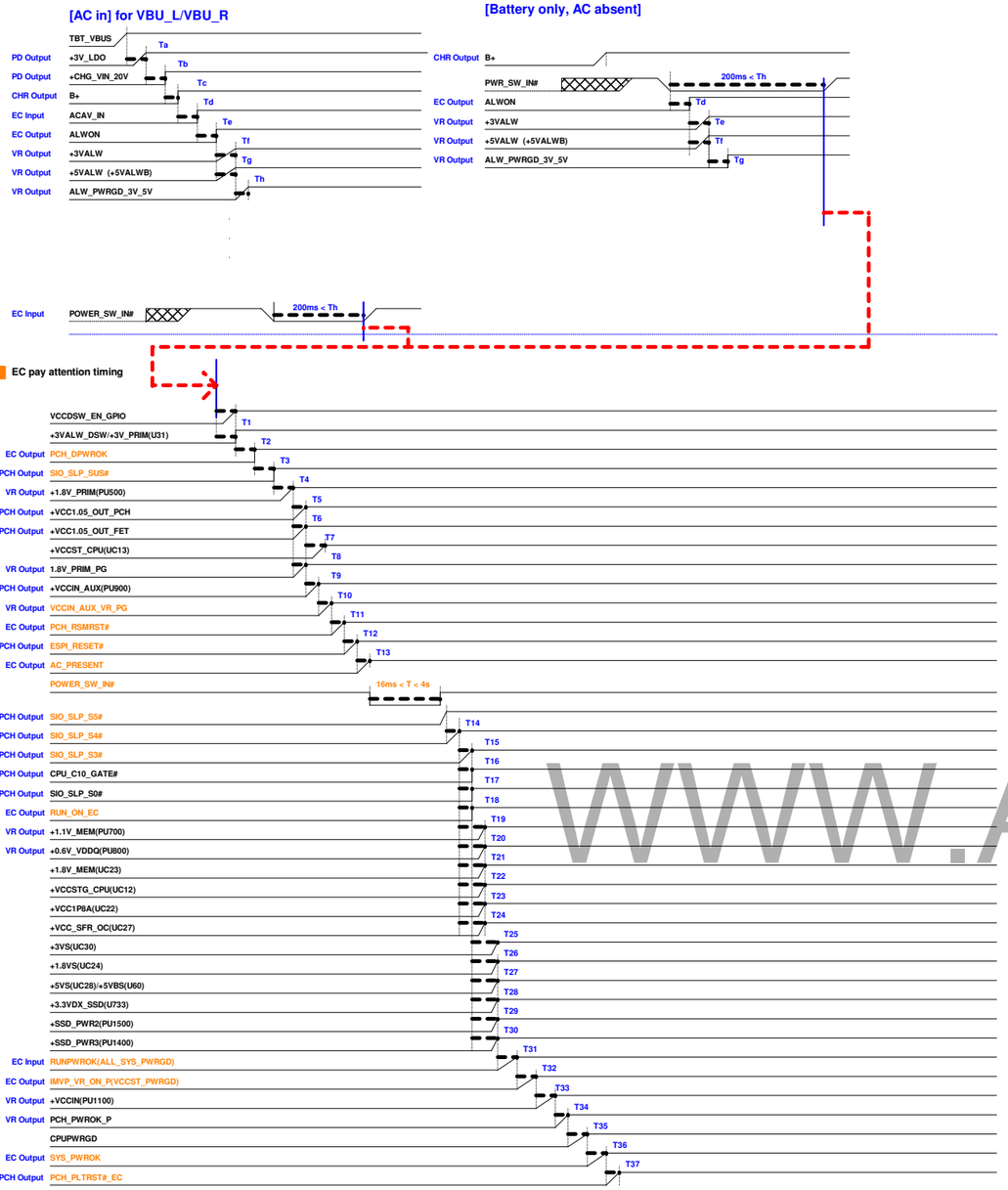
ITEM	Measure Point			Time
Tc	B+	To	POWER_SW_IN#	
Th	POWER_SW_IN#		Low pluse width	
Td	POWER_SW_IN#	To	ALWON	
Te	ALWON	To	+3VALW	
Tf	ALWON	To	+5VALW (+5VALWB)	
Tg	+3VALW	To	ALW_PWRGD_3V_5V	

ITEM	Measure Point			Time
T1	VCCDSW_EN_GPIO	To	+3VALW_DSW/+3V_PRIM	
T2	+3VALW_DSW/+3V_PRIM	To	PCH_DPWROK	
T3	PCH_DPWROK	To	SIO_SLP_SUS#	
T4	SIO_SLP_SUS#	To	+1.8V_PRIM	
T5	+1.8V_PRIM	To	+VCC1.05_OUT_PCH	
T6	+1.8V_PRIM	To	+VCC1.05_OUT_FET	
T7	+VCC1.05_OUT_FET	To	+VCCST_CPU	
T8	+1.8V_PRIM	To	1.8V_PRIM_PG	
T9	1.8V_PRIM_PG	To	+VCCIN_AUX	
T10	+VCCIN_AUX	To	VCCIN_AUX_VR_PG	
T11	VCCIN_AUX_VR_PG	To	PCH_RSMRST#	
T12	PCH_RSMRST#	To	ESPI_RESET#	
T13	ESPI_RESET#	To	AC_PRESENT	
T14	SIO_SLP_S5#	To	SIO_SLP_S4#	
T15	SIO_SLP_S4#	To	SIO_SLP_S3#	
T16	SIO_SLP_S4#	To	CPU_C10_GATE#	
T17	SIO_SLP_S4#	To	SIO_SLP_S0#	
T18	SIO_SLP_S4#	To	RUN_ON_EC	
T19	SIO_SLP_S4#	To	+1.1V_MEM	
T20	SIO_SLP_S4#	To	+0.6V_VDDQ	
T21	SIO_SLP_S4#	To	+1.8V_MEM	
T22	SIO_SLP_S4#	To	+1.8V_MEM	
T23	SIO_SLP_S4#	To	+VCC1P8A	
T24	SIO_SLP_S4#	To	+VCC_SFR_OC	
T25	RUN_ON_EC	To	+3VS	
T26	RUN_ON_EC	To	+1.8VS	
T27	RUN_ON_EC	To	+5VS/+5VBS	
T28	RUN_ON_EC	To	+3.3VDX_SSD	
T29	RUN_ON_EC	To	+SSD_PWR2	
T30	RUN_ON_EC	To	+SSD_PWR3	
T31	+3VS	To	RUNPWROK	
T32	RUNPWROK	To	IMVP_VR_ON_P	
T33	IMVP_VR_ON_P	To	+VCCIN	
T34	+VCCIN	To	PCH_PWROK_P	
T35	PCH_PWROK_P	To	CPUPWRGD	
T36	CPUPWRGD	To	SYS_PWROK	
T37	SYS_PWROK	To	PCH_PLTRST#_EC	

Power Down Sequence

EC pay attention timing

PCH_PLTRST#
CPUPWRGD
PCH_CLK_OUTPUTS
SIO_SLP_S3#
CPU_C10_GATE#
SYS_PWROK
PCH_PWROK_P
IMVP_VR_ON_P(VCCST_PWRGD)
RUNPWROK(ALL_SYS_PWRGD)
+VCCIN
3VS/+1.8VS/+5VS/+5VBS
+VCCSTG_CPU
SIO_SLP_S4#
+1.1V_MEM
+0.6V_VDDQ
+1.8V_MEM
+VCC_SFR_OC
SIO_SLP_S5#
+VCC1P05_OUTPUT_PLL
PCH_RSMRST#
PCH_DPWROK
+3VALW_DSW/+3V_PRIM
SIO_SLP_SUS#
ESPI_RESET#
SIO_SLP_S0#
+1.8V_PRIM
+VCC1.05_OUT_PCH
+VCCIN_AUX
+VCCST_CPU
SUSCLK



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			Date: Friday, May 24, 2019 Sheet 5 of 101

PVT_10

DVT1_76

+3V_PRIM

DVT1_30

10K_0201_5% 2 1 RH742 USB_OC1#

10K_0201_5% 2 1 RH603 USB_OC2#

100K_0201_5% 2 1 RH675 EDP_HPD

100K_0201_5% 2 @ 1 RH717 CPU_TCP0_HPD

100K_0201_5% 2 @ 1 RH718 USB_OC1#

DVT1_30

UC1A

eDP

(38) EDP_TXN0 — Y5 DDIA_TXN_0
(38) EDP_TXP0 — Y3 DDIA_TXP_0
(38) EDP_TXN1 — Y1 DDIA_TXN_1
(38) EDP_TXP1 — Y2 DDIA_TXP_1
(38) EDP_TXN2 — V2 DDIA_TXN_2
(38) EDP_TXP2 — V1 DDIA_TXP_2
(38) EDP_TXN3 — V3 DDIA_TXN_3
(38) EDP_TXP3 — V5 DDIA_TXP_3

(38) EDP_AUXN — W4 DDIA_AUX_N
(38) EDP_AUXP — W3 DDIA_AUX_P

DDI

AE3 DDIB_TXN_0
AE5 DDIB_TXP_0
AE2 DDIB_TXN_1
AE1 DDIB_TXP_1
AC5 DDIB_TXN_2
AC3 DDIB_TXP_2
AC1 DDIB_TXN_3
AC2 DDIB_TXP_3

AD3 DDIB_AUX_N
AD4 DDIB_AUX_P

DP15 — DJ17 GPP_E22/DDPA_CTRLCLK/PCIE_LNK_DOWN / GPP_E23/DDPA_CTRLDATA/BK4/SBK4
DL40 — DP42 GPP_H16/DDPB_CTRLCLK / GPP_H17/DDPB_CTRLDATA

(46) TBT_0_LSX_TX — TBT_0_LSX_RX (46) — DL17 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD / DK17 GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

TBT_1_LSX_RX — DN17 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD / DP17 GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

(48) TBT_2_LSX_TX — TBT_2_LSX_RX (48) — DK34 GPP_D9/ISH_SPI_CS_N/DDP3_CTRLCLK/GSPI2_CS0_N/TBT_LSX2_TXD / DL34 GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/GSPI2_CLK/TBT_LSX2_RXD

TBT_3_LSX_RX — DN33 GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/GSPI2_MISO/TBT_LSX3_TXD / DL33 GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/GSPI2_MOSI/TBT_LSX3_RXD

(38,58) EDP_HPD — EDP_HPD — DW11 GPP_E14/DPPE_HPDA/DISP_MISCA
CV42 GPP_A18/DDSP_HPDB/DISP_MISCB
CPU_TCP0_HPD — CV39 GPP_A19/DDSP_HPD1/DISP_MISC1
CV43 GPP_A20/DDSP_HPD2/DISP_MISC2
DVT1_30 USB_OC1# — CR41 GPP_A14/USB_OC1_N/DDSP_HPD3/DISP_MISC3
USB_OC2# — CT41 GPP_A15/USB_OC2_N/DDSP_HPD4/DISP_MISC4
(38) TS_INT# — DV14 GPP_E17

(38) ENVDD_PCH — DN21 EDP_VDDEN
(10,58) PANEL_BKLEN — DL19 EDP_BKLTEN
(38) EDP_BIA_PWM — DU19 EDP_BKLTCTL
TP99 1 PAD-DTP@ RSVD_1 — J5 RSVD_1
TP69 1 PAD-DTP@ DISP_UTILS — D2 DISP_UTILS
150_0201_1% 2 1 RC3 DP_RCOMP — R2 DISP_RCOMP

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ICL-U_BGA1526

@

TBT / USB / DP

TCP0_TX_N0 BB5 — (46) TBT_0_TTX_DRX_N0
TCP0_TX_P0 BB6 — (46) TBT_0_TTX_DRX_P0
TCP0_TX_N1 AV6 — (46) TBT_0_TTX_DRX_N1
TCP0_TX_P1 AV5 — (46) TBT_0_TTX_DRX_P1
TCP0_TXRX_N0 BH2 — (46) TBT_0_TRX_DTX_N0
TCP0_TXRX_P0 BH1 — (46) TBT_0_TRX_DTX_P0
TCP0_TXRX_N1 BF1 — (46) TBT_0_TRX_DTX_N1
TCP0_TXRX_P1 BF2 — (46) TBT_0_TRX_DTX_P1
TCP0_AUX_N AY5 — (46) TBT_0_DP_AUXN
TCP0_AUX_P AY6 — (46) TBT_0_DP_AUXP

TBT_L

TCP1_TX_N0 AR5
TCP1_TX_P0 AR6
TCP1_TX_N1 AL5
TCP1_TX_P1 AL3
TCP1_TXRX_N0 BD2
TCP1_TXRX_P0 BD1
TCP1_TXRX_N1 BB1
TCP1_TXRX_P1 BB2
TCP1_AUX_N AN3
TCP1_AUX_P AN5

TCP2_TX_N0 BF6 — (48) TBT_2_TTX_DRX_N0
TCP2_TX_P0 BF5 — (48) TBT_2_TTX_DRX_P0
TCP2_TX_N1 BJ5 — (48) TBT_2_TTX_DRX_N1
TCP2_TX_P1 BJ6 — (48) TBT_2_TTX_DRX_P1
TCP2_TXRX_N0 BL1 — (48) TBT_2_TRX_DTX_N0
TCP2_TXRX_P0 BL2 — (48) TBT_2_TRX_DTX_P0
TCP2_TXRX_N1 BM2 — (48) TBT_2_TRX_DTX_N1
TCP2_TXRX_P1 BM1 — (48) TBT_2_TRX_DTX_P1
TCP2_AUX_N BG6 — (48) TBT_2_DP_AUXN
TCP2_AUX_P BG5 — (48) TBT_2_DP_AUXP

TBT_R

TCP3_TX_N0 BP6
TCP3_TX_P0 BP5
TCP3_TX_N1 BV5
TCP3_TX_P1 BV6
TCP3_TXRX_N0 BR1
TCP3_TXRX_P0 BR2
TCP3_TXRX_N1 BT2
TCP3_TXRX_P1 BT1
TCP3_AUX_N BT6
TCP3_AUX_P BT5

TC_RCOMP_N AY1 — TCRCOMP_DN RC1 1 2 150_0201_1%
TC_RCOMP_P AY2 — TCRCOMP_DP

GPP_A17/DISP_MISCC CT38 — RTC_DET# 1 @ 2 RH734 0_0201_5% — RTC_DET#_R (63)
GPP_A21 CV43 — 3.3V_CAM_EN (71)
GPP_A22 CV41 — KB_DET# (63)

DVT1_62

+3V_PRIM

KB_DET# RH6721 2 10K_0201_5%

+3V_PRIM

R6172 @ 4.7K_0201_5% — TBT_0_LSX_RX — RC691 20K_0201_5%

TBT LSX #0 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

+3V_PRIM

R6173 @ 4.7K_0201_5% — TBT_1_LSX_RX — RC692 @ 20K_0201_5%

TBT LSX #1 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

+3V_PRIM

R6174 @ 4.7K_0201_5% — TBT_2_LSX_RX — RC693 20K_0201_5%

TBT LSX #2 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

+3V_PRIM

R6175 @ 4.7K_0201_5% — TBT_3_LSX_RX — RC694 @ 20K_0201_5%

TBT LSX #3 PINS VCCIO CONFIGURATION	
HIGH	3.3V
LOW	1.8V

PLACE CLOSE TO THE SIGNAL TO AVOID STUB

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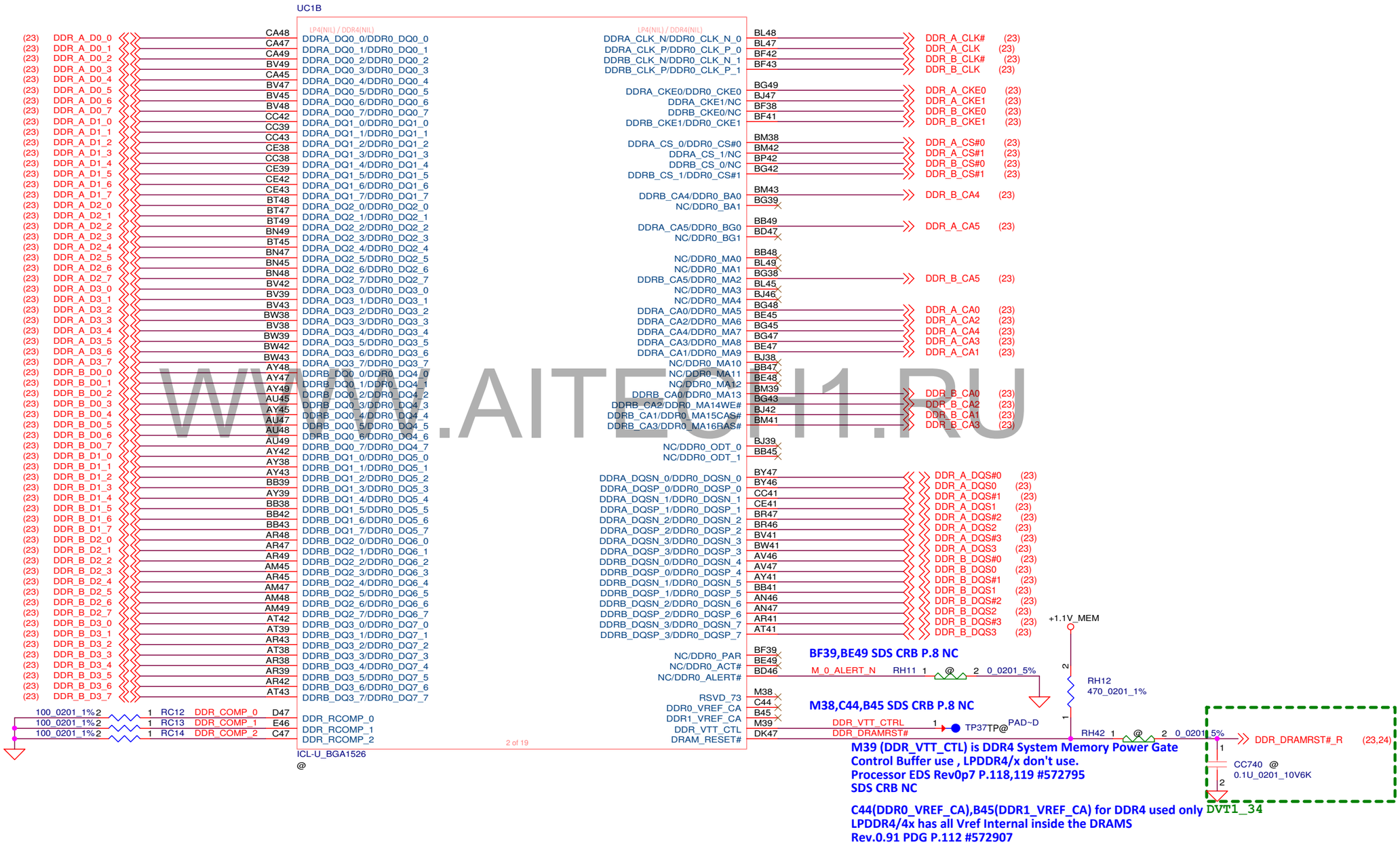
Issued Date	2015/10/22	Deciphered Date 2013/10/28	Title: P006 - ICL-U(1/13)TCSS,EDP
			Size: LA-G172P; Document Number; Rev 1.0 (A00)
			Date: Friday, May 24, 2019; Sheet 6 of 101

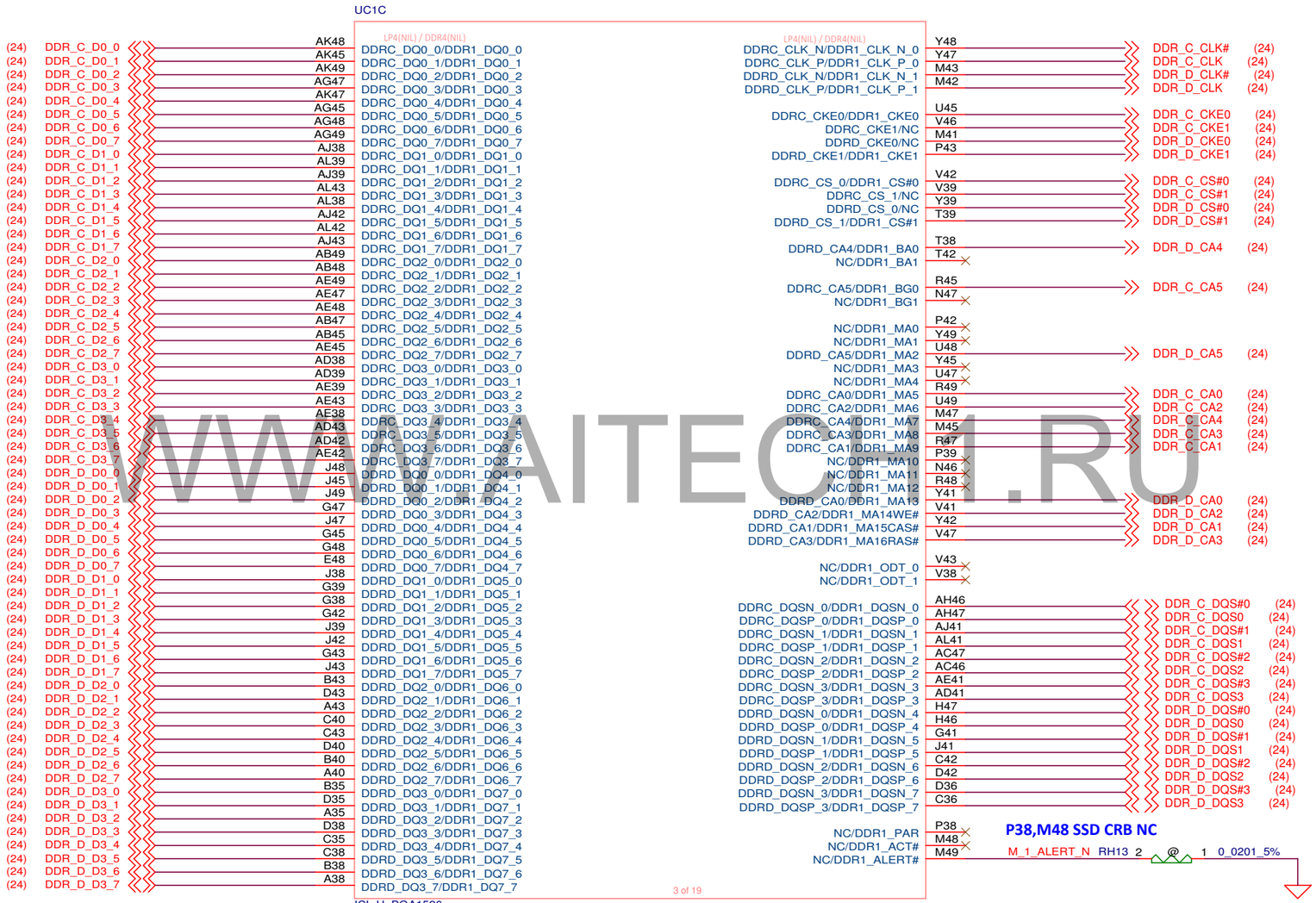
Memory connection follow J72913-201 Rev 01_20181217



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P007 - ICL-U(2/13)LPDDR4/x			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 7 of 101		

Memory connection follow J72913-201 Rev 01_20181217



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P008 - ICL-U(3/13)LPDDR4/x
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date: Friday, May 24, 2019	Sheet 8 of 101

BOOT HALT

SPI0_MOSI(NO INTERNAL PU/PD)

0 = Enable

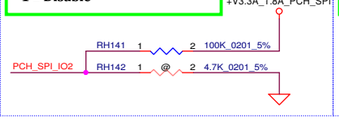
1 = Disable

CONSENT STRAP

SPI0_IO2(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

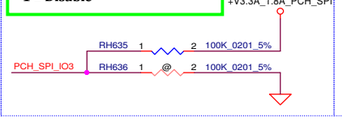


A0 PERSONALITY STRAP

SPI0_IO3

0 = Enable

1 = Disable

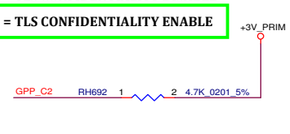


TLS CONFIDENTIALITY

GPP_C2/SMBALERT#(INTERNAL PD 20K)

0 = TLS CONFIDENTIALITY DISABLE

1 = TLS CONFIDENTIALITY ENABLE

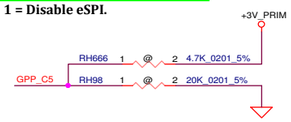


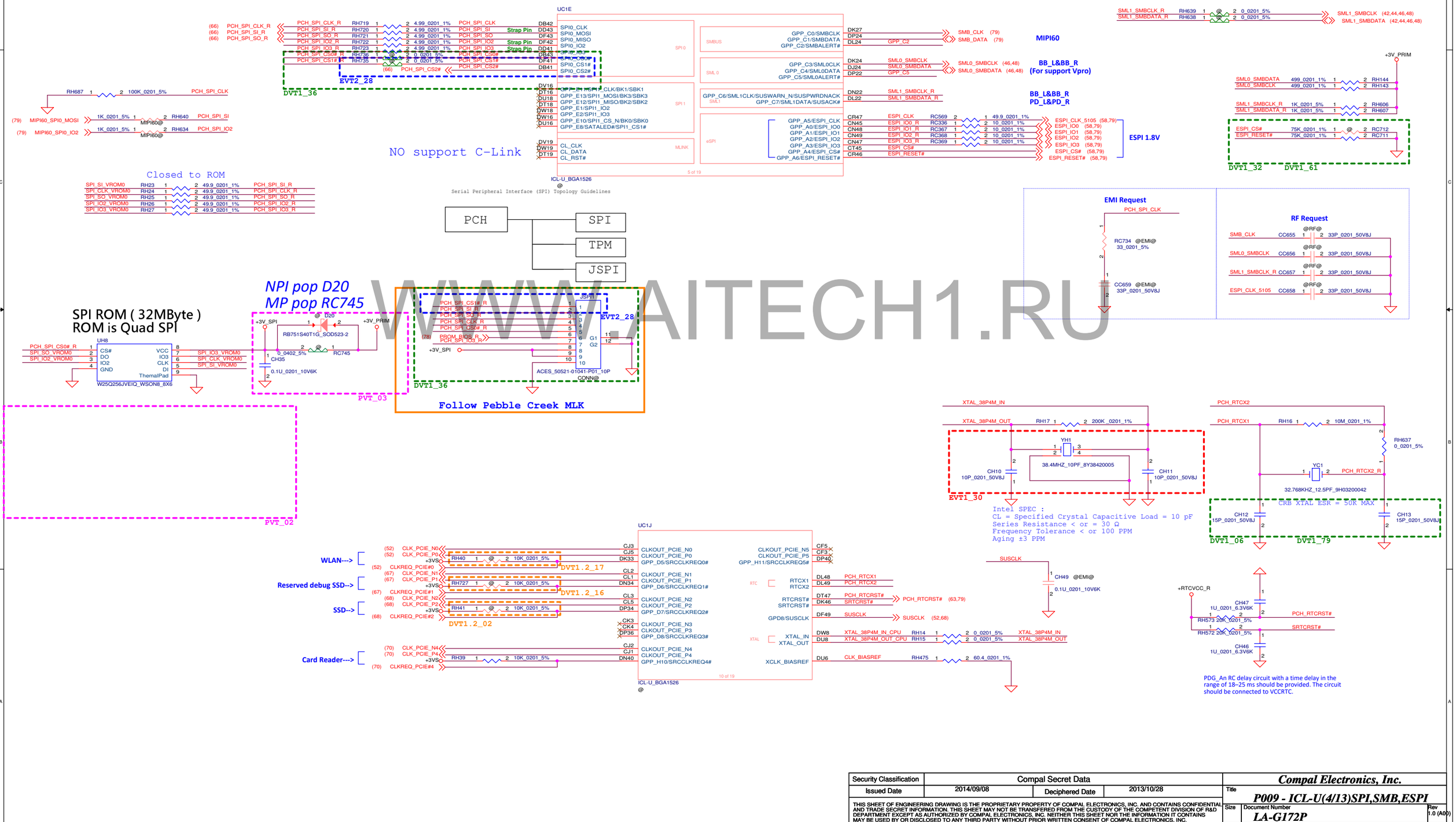
ESPI OR EC LESS

GPP_C5 (Internal 20 K internal Pull Down): SML0ALERT#

0 = Enable eSPI. (Default)

1 = Disable eSPI.





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	P009 - ICL-U(4/13)SPI,SMB,ESPI
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
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NO REBOOT

GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

0 = REBOOT ENABLED

1 = NO REBOOT

CPUNSSC CLOCK FREQ

GPP_B23 (Internal 20 K Pull Down)

0 = 38.4 MHz clock (direct from crystal) (default)

1 = 19.2 MHz clock (from internal divider)

TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

FLASH DESCRIPTOR SECURITY OVERRIDE

GPP_R2/HDA_SDO (Internal 20 K Pull Down)

0 = ENABLE (DEFAULT)

1 = DISABLE (ME can update)

For TS lid open reserved

TS

TP

Reserved

UFCAM

EC

2nd Accelerometer

ALS,Ecompass,Main Accelerometer on SDB.
Ecompass,Main Accelerometer on DB.

Reserved for debug

Intel DMIC for WOV reserved

HDA for AUDIO

RF Request. Place near CPU side

CPU I3/I5/I7 Option for different thermal table

Pin Name	I3	I5	I7
CPU_ID_0	0	0	1
CPU_ID_1	0	1	0

ISH_GP0 for Main Accelerometer (Sensor Board)INT1#
ISH_GP1 for 2nd Accelerometer (MB)
ISH_GP2 for Main Accelerometer (Sensor Board)INT2#
ISH_GP3 for NB_MODE
ISH_GP4 for ISH_GP4# (ON TABLE)
ISH_GP5 for NB_LID#
ISH_GP6 for TAB_LID#
ISH_GP7 for ALS_ALERT#

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
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Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
Sheet	10 of 101

3V SELECT STRAP

INPUT3VSEL

0 = 3.3V +/-5%

1 =3.0V +/-5%

+3VALW_DSW

RH301 1 @ 2 4.7K_0201_5%

INPUT3VSEL — RH298 1 2 100K_0201_5%

STRAP FOR SPI 1.8V/3.3V SEL

INTRUDER#

0 = SPI voltage is 3.3V

1 = SPI voltage is 1.8V

+RTCVCC

1M_0201_1% 2 @ 1 RH64 — INTRUDER#

10K_0201_1% 2 @ 1 RH671

0.1U_0201_10V6K 2 @ 1 CC653

DVT1_81

Microchip suggest 100K on RH575

2 1 PCH_DPWROK

1M_0201_1% — RH575

2 1 @ CH48

0.01U_0402_16V7K

UC1K

(16,47,49,58) SIO_SLP_SUS# — SIO_SLP_SUS# DM49 — SLP_SUS#

(79) SIO_SLP_S5# — SIO_SLP_S5# DF45 — GPD10/SLP_S5#

(58,78,79) SIO_SLP_S4# — SIO_SLP_S4# DC48 — GPD5/SLP_S4#

(58,78,79) SIO_SLP_S3# — SIO_SLP_S3# DF47 — GPD4/SLP_S3#

(79) SIO_SLP_A# — SIO_SLP_A# DH47 — GPD6/SLP_A#

(66,79) SIO_SLP_S0# — SIO_SLP_S0# CL45 — GPP_B12/SLP_S0#

GPP_H3/SX_EXIT_HOLDOFF_N/CNV_BT_I2S_SDO

(71) SIO_SLP_WLAN# — SIO_SLP_WLAN# DE49 — GPD9/SPL_WLAN#

DN48 — SLP_LAN#

(63,78) PCH_RSMRST#_AND — PCH_RSMRST#_AND DG49 — RSMRST#

(79) SYS_RESET# — SYS_RESET# DK19 — SYS_RESET#

PCH_PLTRST# CM49 — GPP_B13/PLTRST#

(58) PCH_DPWROK — PCH_DPWROK DR48 — DSW_PWROK

PCH_PWROK DN47 — PCH_PWROK

(58,79) SYS_PWROK — SYS_PWROK 0_0201_5% 2 @ 1 RH594 SYS_PWROK_R DP19 — SYS_PWROK

INPUT3VSEL DN49 — INPUT3VSEL

INTRUDER# Strap Pin DR47 — INTRUDER#

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ICL-U_BGA1526

@

GPD3/PWRBTN# — CY42 SIO_PWRBTN#_R RH57 1 @ 2 0_0201_5% — SIO_PWRBTN# (58,79)

GPD1/ACPRESENT — DE46 AC_PRESENT_R RH312 1 @ 2 0_0201_5% AC_PRESENT — AC_PRESENT (58)

GPD0/BATLOW# — DH48 PCH_BATLOW#

GPP_B11/PMCALERT# — CL39 GPP_B11 RH659 1 @ 2 0_0201_5% TBT_I2C_INT# — TBT_I2C_INT# (42,44,46,48)

GPP_H18/CPU_C10_GATE# — DU40 CPU_C10_GATE#_R RH280 1 @ 2 0_0201_5% — CPU_C10_GATE# (78)

DG40 GPP_H3 — 1 TP57 PAD~D TP@

WAKE# — DL45 WAKE# RH207 1 @ 2 0_0201_5% — PCH_PCIE_WAKE# (58)

GPD2/LAN_WAKE# — DE47 LAN_WAKE#_R RH600 1 @ 2 0_0201_5% LAN_WAKE# — LAN_WAKE# (58)

GPD11/LANPHYPC/DSWLDO_MON — DF48

VCCST_OVERRIDE — CE4 VCCST_OVERRIDE

VCCST_PWRGD — CF2 VCCST_PWRGD_CPU RH5871 2 60.4_0201_1% VCCST_PWRGD — VCCST_PWRGD (78)

VCCSTPWRGOOD_TCSS — CE3 VCCSTPWRGOOD_TCSS

PROCPWRGD — CF1 CPUPWRGD 1 @ 2 CPUPWRGD_R 1 — TP70 PAD~D TP@

RH595 1K_0201_5%

GPD7 — DC47 GPD7 — 1 TP101 PAD~D TP@

+3V_PRIM

PCH_RSMRST#_AND — RH592 1 @ 2 10K_0201_5%

TBT_I2C_INT# — RC687 1 2 10K_0201_5%

PCH_RSMRST#_AND — RH591 1 2 100K_0201_5%

+3VALW_DSW

LAN_WAKE# — RH601 1 2 10K_0201_5%

PCH_BATLOW# — RH460 1 2 100K_0201_5%

AC_PRESENT — RH297 1 2 10K_0201_5%

PCH_PCIE_WAKE# — RH653 1 2 1K_0201_5%

DVT1_41

(78) VCCST_OVERRIDE_R — VCCST_OVERRIDE_R 0_0201_5% 2 @ 1 RH584 VCCST_OVERRIDE

0_0201_5% 2 @ 1 RH586 VCCSTPWRGOOD_TCSS

(79) PM_RSMRST_PWRGD_MIPI60 — 1K_0201_5% 2 @ 1 RC647 VCCST_PWRGD

1K_0201_5% 2 MIPI60@ 1 RC247 PCH_RSMRST#_AND

PLACE 1K SERIES RESISTOR NEAR RSMRST_N AND VCCST_PWRGD

"T" JUNCTION POINT, NOT NEAR MIPI60

if pop UC29, RC244 also need pop

RC430 1 @ 2 0_0201_5%

(79) MIPI60_DBRESET#_R

+3VS — RC433 1 @ 2 8.2K_0201_5% ME_RESET# 2

RC434 1 @ 2 8.2K_0201_5%

UC29 @ — +3VS — CC77 @ 2 1 — 0.1U_0201_10V6K

1 B 5 — 4 SYS_RESET#_R 2 — RC432

A O

3 — MC74VHC1G08DFT2G_SC70-5

DVT1_28

+3VS — RC244 @ 10K_0201_5% — SYS_RESET# — 1K_0201_5%

VCCST_PWRGD — CC649 EMI@ 1 2 100P_0201_50V8J

CPUPWRGD — CC650 EMI@ 1 2 100P_0201_50V8J

SYS_RESET# — CC651 @EMI@ 1 2 0.1U_0201_10V6K

ESD Request:place near CPU side

+3VS — RH733 100K_0201_5%

RH625 1 @ 2 0_0201_5%

+3VS — UH6 @

(91) PCH_PWROK_P — 1 B 5 — 4 PCH_PWROK

(78) IMVP_VR_ON_P — 2 A O — MC74VHC1G08DFT2G_SC70-5

3

DVT1_28

+1.05V_VCCST

RH95 2 1 1K_0201_1% H_THERMTRIP#

RH80 2 1 49.9_0201_1% H_CATERR#

RH588 2 1 1K_0201_5% VCCST_PWRGD

PLACE "RA" CLOSE TO MCP - WITHIN 1.5 INCH CRB P.35

+1.05V_VCCSTG

RH96 2 1 1K_0201_5% H_PROCHOT#

+3VS

RH631 1 2 10K_0201_5% PCH_TOUCHPAD_INTR#

+3V_PRIM

RH709 1 2 100K_0201_5% SIO_SLP_S0#

UC1D

(58) PECI_EC — H_CATERR# — J4 CATERR# — PROC_TCK — P3 — MIPI60_CPU_JTAG_TCLK

PECI_EC — CD5 PECI — PROC_TDI — K5 — MIPI60_CPU_JTAG_TDI (79)

(16,58,91) H_PROCHOT# — H_PROCHOT#_R RC614 1 2 499_0201_1% — C3 PROCHOT# — PROC_TDO — K3 — MIPI60_CPU_JTAG_TDO (79)

(58) H_THERMTRIP# — H_THERMTRIP# — E3 THRMTRIP# — PROC_TMS — P4 — MIPI60_CPU_JTAG_TMS (79)

PROC_TRST# — N1 — MIPI60_CPU_JTAG_TRST# (79)

PROC_POPIRCOMP

PCH_OPIRCOMP — JTAG

RSVD_25

RSVD_26

RH4 2 1 49.9_0201_1% CPU_POPI_RCOMP — CJ41

RH5 2 1 49.9_0201_1% PCH_OPI_RCOMP — DU3

RH6 2 1 49.9_0201_1% EDRAM_OPIO_RCOMP — A14

RH7 2 1 49.9_0201_1% CPU_EOPIO_RCOMP — B14

(79) DBG_PMODE — Strap Pin DL15 — DBG_PMODE

MEM_INTERLEAVED — DV11

TOUCH_SCREEN_PD# — DT11

(63) PCH_TOUCHPAD_INTR# — PCH_TOUCHPAD_INTR# — CR38

CR39

GPP_E6 — Strap Pin DT12

GPP_H2 — Strap Pin DJ38

DL38

GPP_E3/CPU_GP0

GPP_E7/CPU_GP1

GPP_B3/CPU_GP2

GPP_B4/CPU_GP3

GPP_E6

GPP_H2/CNV_BT_I2S_SDO

GPP_H19/TIME_SYNCO

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ICL-U_BGA1526

@

PCH_PLTRST# — RH5 2 1 49.9_0201_1% PCH_PLTRST# — DU3

PROC_PRDY# — P6 — MIPI60_PRDY# (79)

PROC_PREQ# — M6 — MIPI60_PREQ# (79)

+3V_PRIM

PCH_PLTRST# — UH1 1 B 5 — 4 PCH_PLTRST#_EC (46,48,52,58,66,67,68,70,79)

2 A O — MC74VHC1G08DFT2G_SC70-5

3

DVT1_28

+3V_PRIM — 2 — CC652 0.1U_0201_10V6K — 1

RH46 100K_0201_5%

DVT1_52

DVT1_43

+3VS

DVT1_46

RH655 @ 100K_0201_5%

(38) TOUCH_SCREEN_PD#_R — @D468 2 1 TOUCH_SCREEN_PD# — RB751S40T1G_SOD523-2

0_0201_5% 2 @ 1 RH654

DVT1_78

DVT1.2_19

RH743 2 @ 1 LID_CL_TS_FP# (58,77)

0_0201_5%

DVT1_04 EVT1_19

+3VALW

RC147 100K_0201_5%

D2 — G2 — S2 — PMDXB600UNE_DFN1018-6 — QC2B

D1 — G1 — S1 — PMDXB600UNE_DFN1018-6 — QC2A

DISPOFF R#

RH744 0_0201_5%

(38) DISPOFF#

DVT1_77

PCH GLITCH ISSUE MITIGATION(PDG p.306)

RH683 1 2 100K_0201_5% — SIO_SLP_S3#

CH53 1 @ 2 0.33U_0201_6.3V6M

RH684 1 2 100K_0201_5% — SIO_SLP_S4#

CH54 1 @ 2 0.33U_0201_6.3V6M

RH685 1 2 100K_0201_5% — SIO_SLP_A#

CH55 1 @ 2 0.33U_0201_6.3V6M

RH682 1 2 100K_0201_5% — SIO_SLP_WLAN#

CH52 1 @ 2 0.33U_0201_6.3V6M

RH686 1 2 100K_0201_5% — SIO_SLP_SUS#

CH56 1 @ 2 0.33U_0201_6.3V6M

RH689 1 @ 2 100K_0201_5% — SIO_SLP_S0#

RH690 1 @ 2 100K_0201_5% — PCH_PLTRST#

RH691 1 @ 2 100K_0201_5% — SIO_SLP_S5#

CH57 1 @ 2 0.33U_0201_6.3V6M

DVT1_32

EMI request,Place near CPU side.

MIPI60_PCH_JTAG_TDO — CC735 @EMI@ 1 2 0.1U_0201_25V6K

MIPI60_PCH_JTAG_TDI — CC736 @EMI@ 1 2 0.1U_0201_25V6K

MIPI60_PCH_JTAGX — CC737 @EMI@ 1 2 0.1U_0201_25V6K

H_THERMTRIP# — CC738 @EMI@ 1 2 0.1U_0201_25V6K

H_PROCHOT#_R — CC739 @EMI@ 1 2 0.1U_0201_25V6K

+3V_PRIM

PCH_PWROK — RH629 1 @ 2 10K_0201_5%

MEM_INTERLEAVED — RH630 1 @ 2 10K_0201_5%

DVT1_63

DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

EVT1_31

+1.05V_VCCSTG

PLACE WITHIN 1.1INCH OF MCP

MIPI60_PCH_JTAG_TDI — RC151 1 MIPI60@2 51_0201_5%

MIPI60_PCH_JTAG_TMS — RC203 1 MIPI60@2 51_0201_5%

MIPI60_PCH_JTAG_TDO — RC202 1 2 100_0201_5%

TDI,TMS KEEP STUB TO WITHIN

MIPI60_CPU_JTAG_TDI — RC146 1 @ 2 51_0201_5%

MIPI60_CPU_JTAG_TMS — RC181 1 @ 2 51_0201_5%

MIPI60_CPU_JTAG_TDO — RC150 1 @ 2 100_0201_5%

TDO PLACE WITHIN 1.1INCH OF SOC

DVT1_50

PLACE WITHIN 1.1INCH OF SOC

MIPI60_CPU_JTAG_TCLK — RC145 1 @ 2 51_0201_5%

MIPI60_PCH_JTAG_TCLK — RC180 1 @ 2 51_0201_5%

MIPI60_PCH_JTAG_TRST# — RC201 1 @ 2 51_0201_5%

MIPI60_PCH_JTAGX — RC344 1 @ 2 51_0201_5%

JTAG ODT DISABLE

GPP_E6

0 = JTAG ODT DISABLED

1 = JTAG ODT ENABLED

+3V_PRIM

GPP_E6 — RH660 1 2 100K_0201_5% — RH661 1 @ 2 4.7K_0201_5%

MAF/SAF STRAP(eSPI Flash Sharing Mode)

GPP_H2/CNV_BT_I2S_SDI(INTERNAL PD 20K)

0 = MAF (Master Attached Flash)

1 = SAF (Slave Attached Flash)

+3V_PRIM

GPP_H2 — RH618 1 @ 2 2.2K_0201_5% — RH617 1 @ 2 20K_0201_5%

EVT2_33

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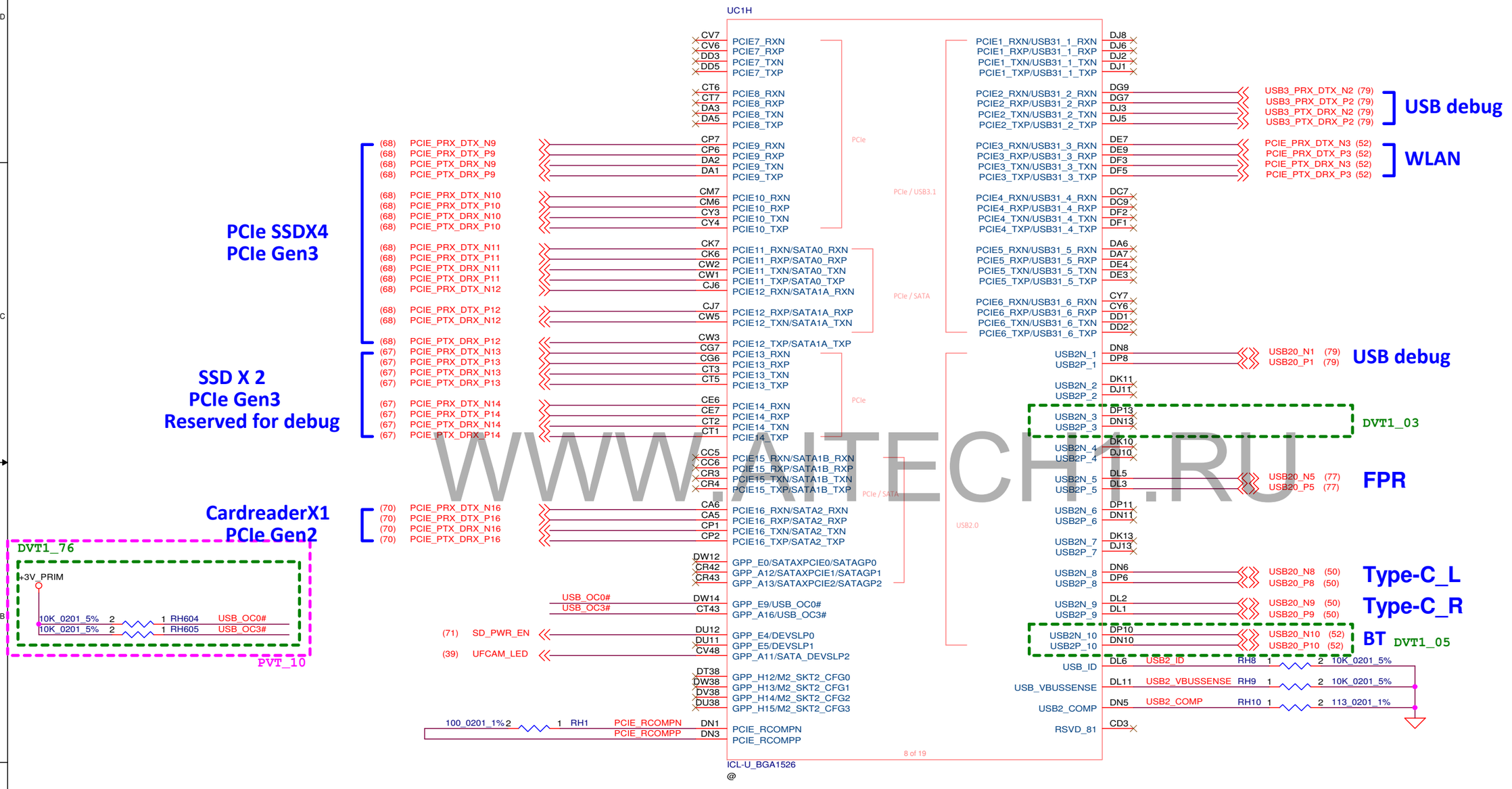
Date: Friday, May 24, 2019 — Sheet 11 of 101



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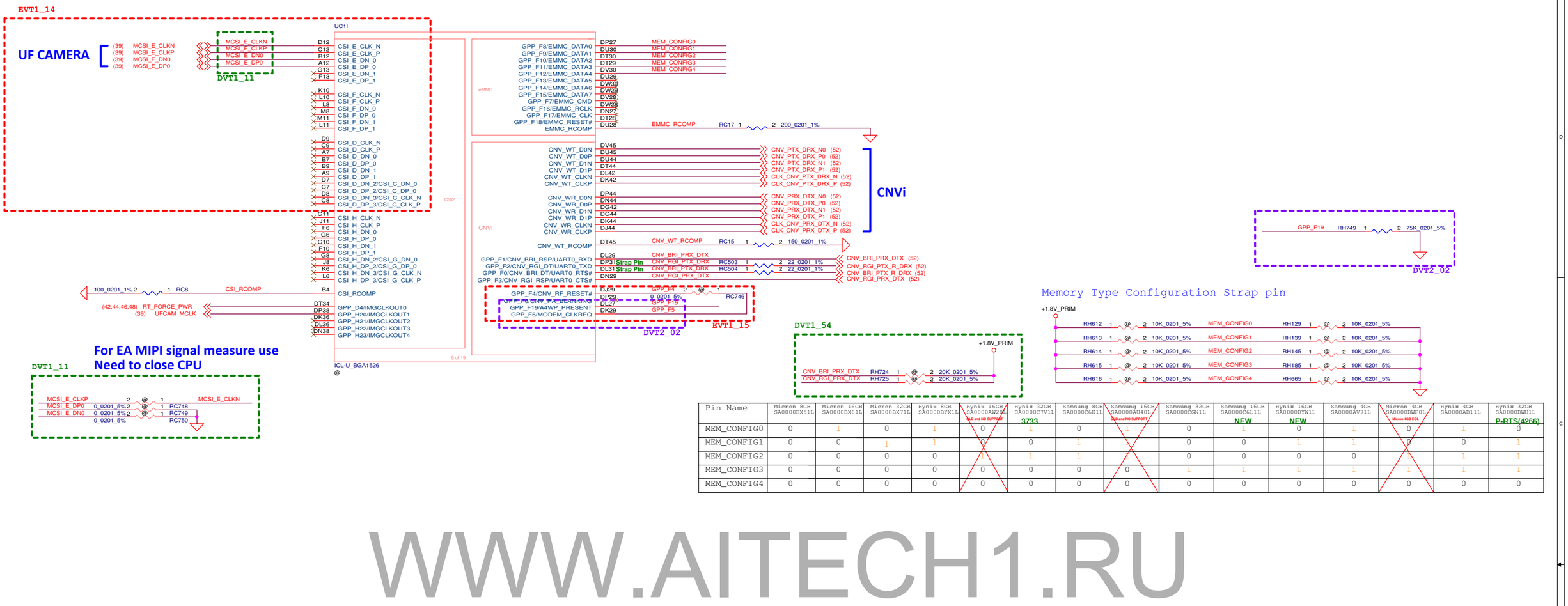
Title	P012 - ICL-U(7/13)PCIE,USB
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
Sheet	12 of 101



Pin Name	Micron 8GB SA0000BX51L	Micron 16GB SA0000BX61L	Micron 32GB SA0000BX71L	Hynix 8GB SA0000BYX1L	Hynix 16GB SA0000AW2YL EOL and NO SUPPORT	Hynix 32GB SA0000C7V1L 3733	Samsung 8GB SA0000C6K1L	Samsung 16GB SA0000AU40L EOL and NO SUPPORT	Samsung 32GB SA0000CGN1L	Samsung 16GB SA0000C6L1L NEW	Hynix 16GB SA0000BYW1L NEW	Samsung 4GB SA0000AV71L	Micron 4GB SA0000BWF0L Micron 4GB EOL	Hynix 4GB SA0000AD11L	Hynix 32GB SA0000BWU1L P-RTS(4266)
MEM_CONFIG0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
MEM_CONFIG2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
MEM_CONFIG3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

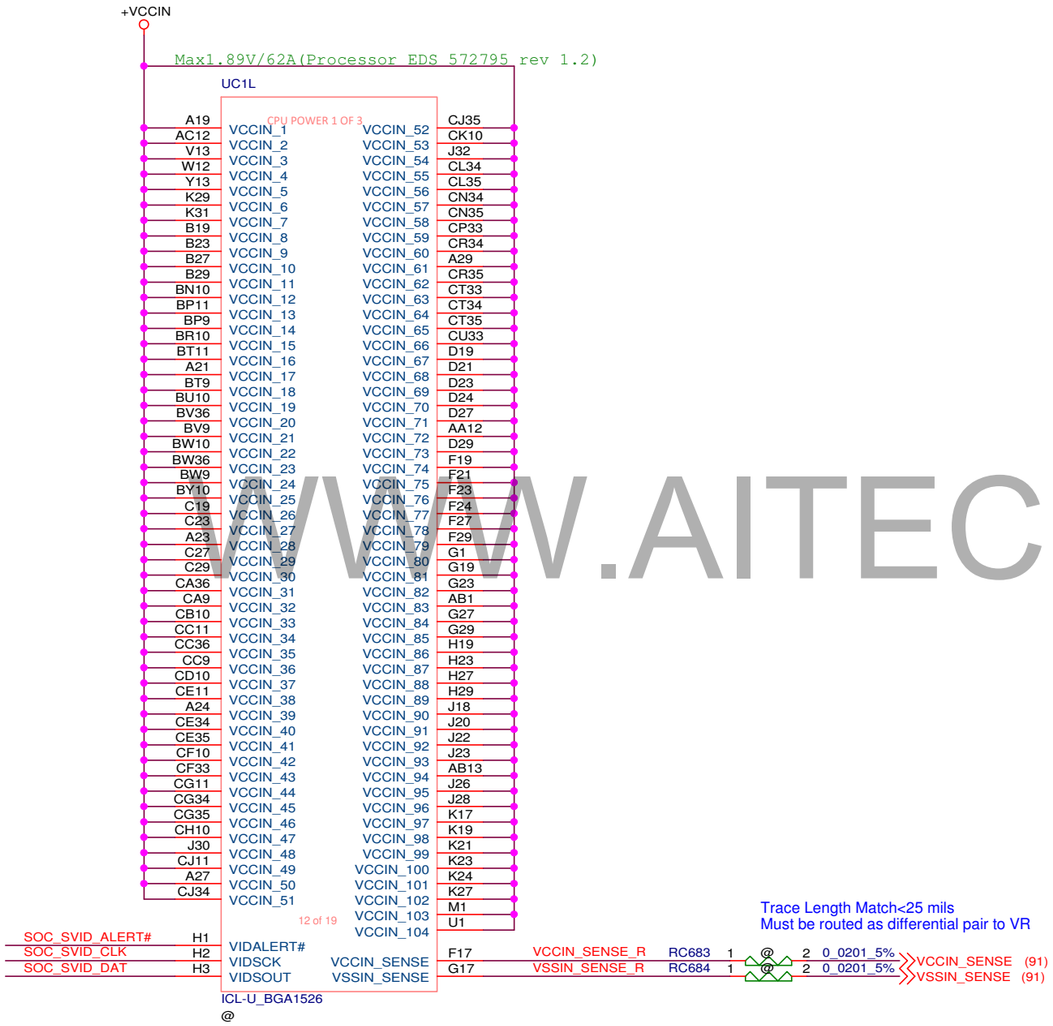
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

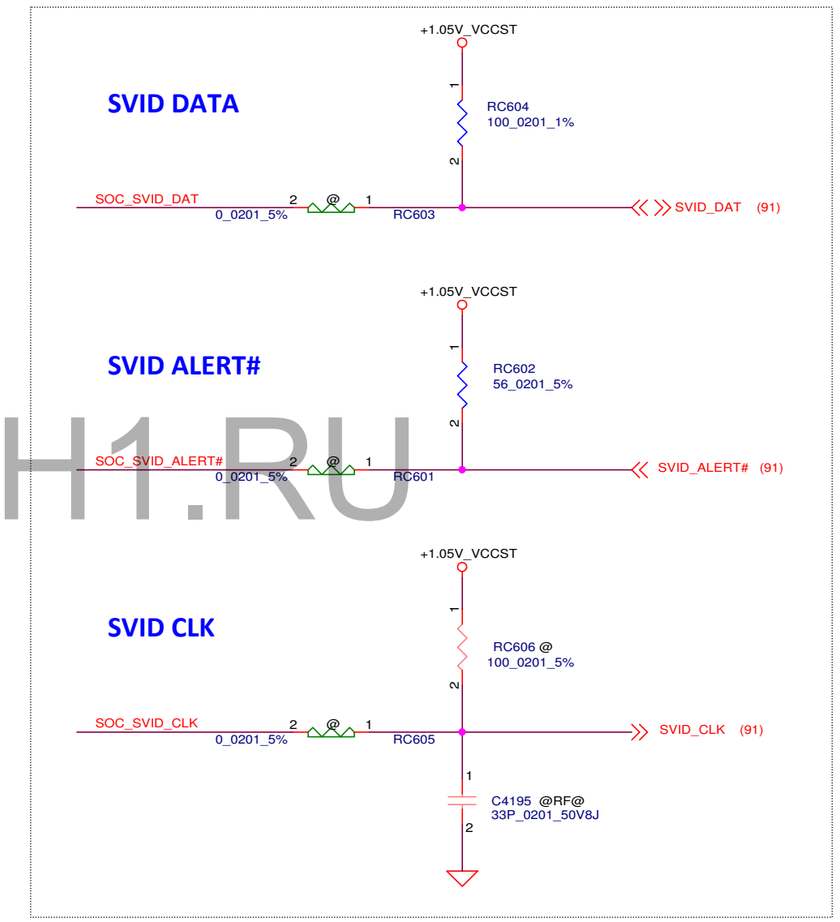
Title: *P013 - ICL-U(8/13)CSI,CNVi,EMMC*

Size | Document Number: *LA-G172P* | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 13 of 101

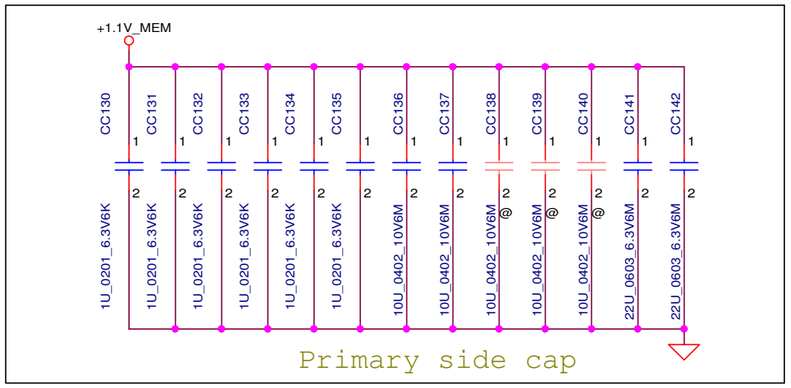


1.The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
2.Route the Alert signal between the Clock and the Data signals.
CAD Note: Place the PU resistors close to CPU

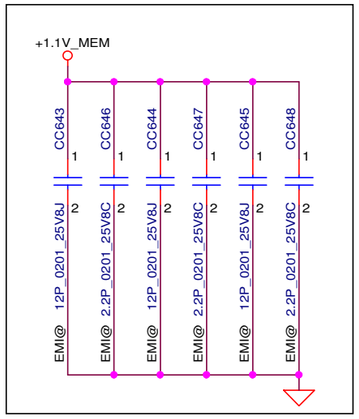


Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

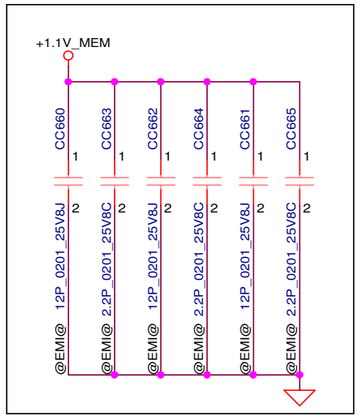
Compal Electronics, Inc.			
Title	P014 - ICL-U(9/13)CPU PWR,SVID		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
Date:	Friday, May 24, 2019	Sheet 14 of 101	

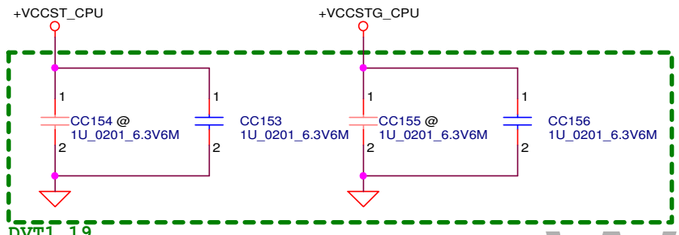


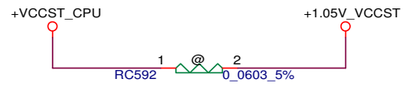
Follow PDG rev1.1 P.545

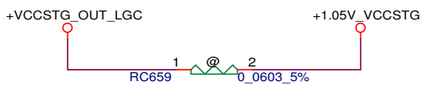


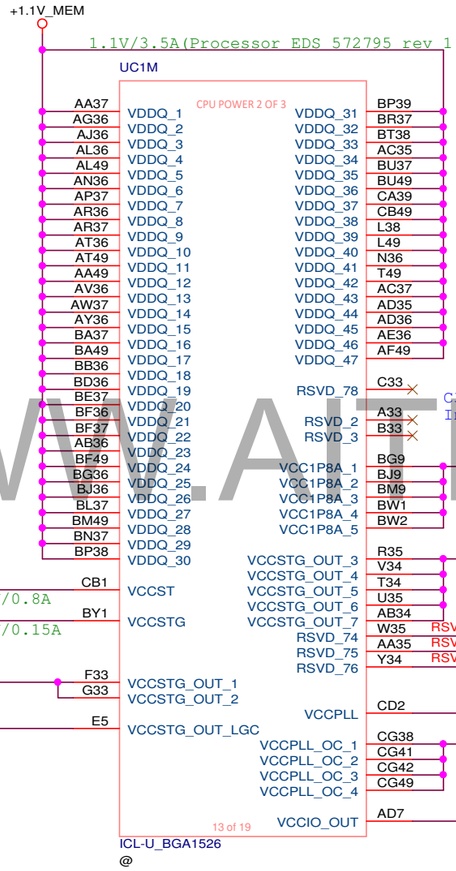
EMC CAPS
PLACE <160mil FROM SOC VDDQ,
WITH EACH PAIR <470mil APART

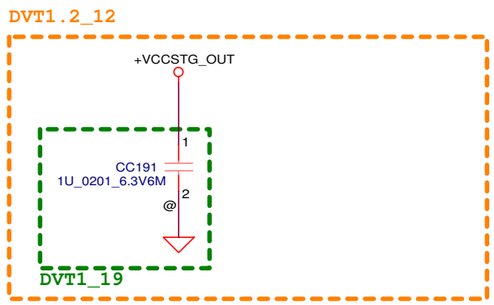


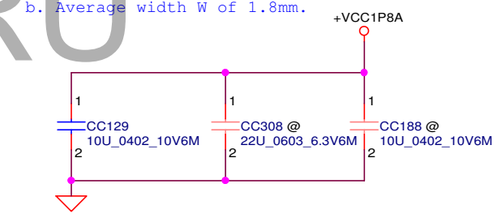


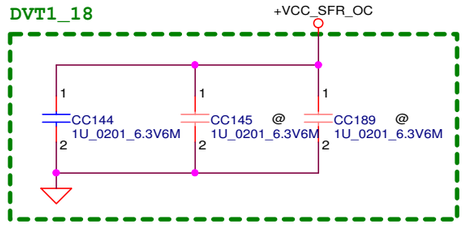


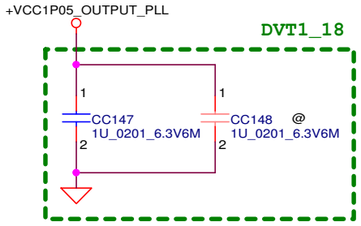












VCC1P8A shape from VR to VCC1P8A pins should have:
a. total length L of < 22mm between VR and BGA.
b. Average width W of 1.8mm.

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P015 - ICL-U(10/13)CPU PWR			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 15 of 101		

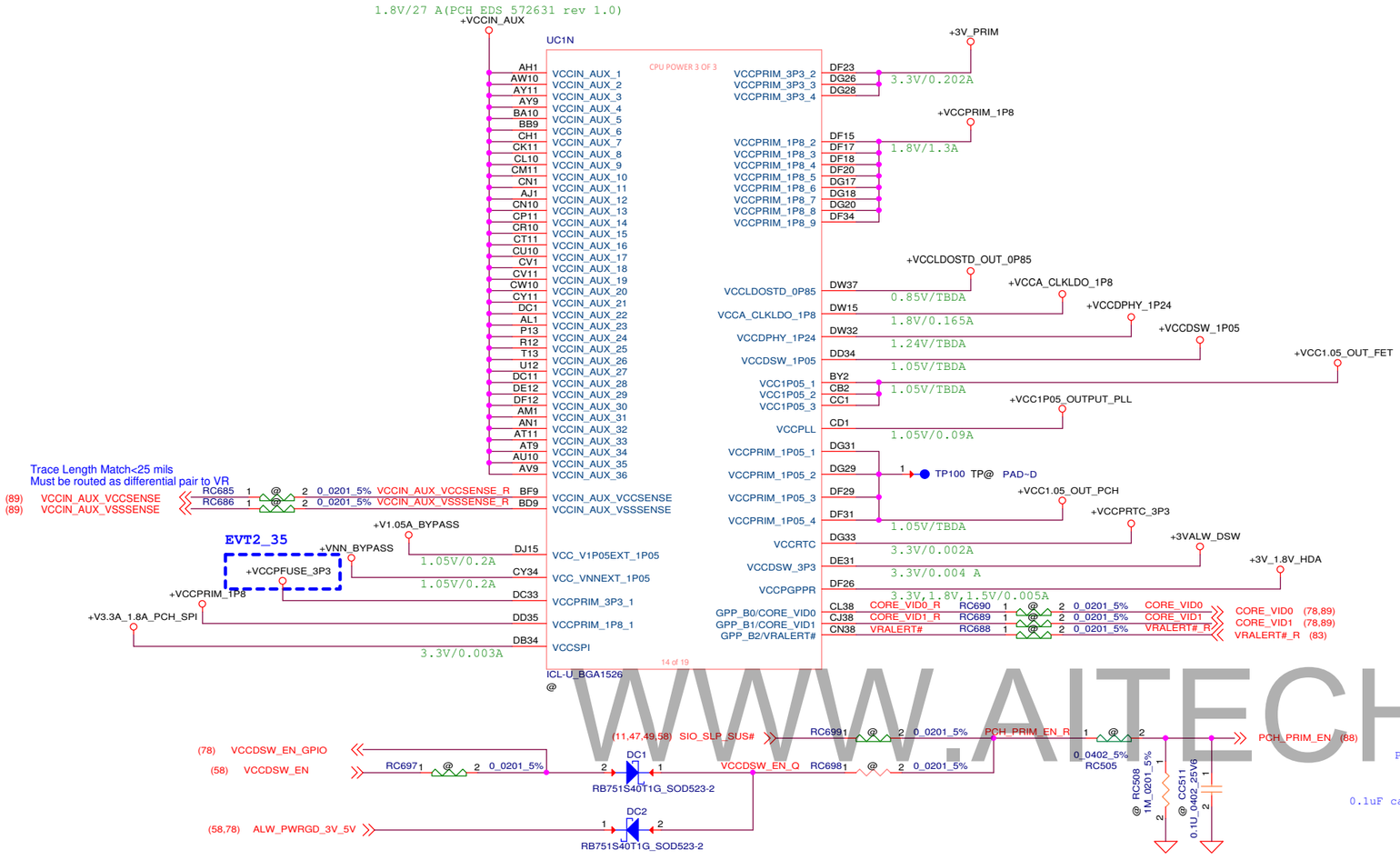


Table 11-1. VCCIN_AUX VID

VID[1] Pin State	VID[0] Pin State	VCCIN_AUX Voltage (V)	Usage
0	0	0	Power Saving State
0	1	1.1	Power Saving State
1	0	1.65	Full Current, ICL-Y
1	1	1.8	Initial boot for ICL-U/Y Full current, ICL-U

Note: Logic "0"is 0V and Logic "1" is 1.8V based logic, but the VID pins must be 3.3V tolerant as well.

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P016 - ICL-U(11/13)PCH Power
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A11	VSS_1	VSS_75	AF45
A46	VSS_2	VSS_76	AF47
BA45	VSS_3	VSS_77	AG1
BA47	VSS_4	VSS_78	AG11
BB11	VSS_5	VSS_79	AG3
BB3	VSS_6	VSS_80	AG38
BB7	VSS_7	VSS_81	AG39
BC37	VSS_8	VSS_82	AG41
BD3	VSS_9	VSS_83	A31
BD38	VSS_10	VSS_84	AG42
BD39	VSS_11	VSS_85	AG43
BD41	VSS_12	VSS_86	AG5
A48	VSS_13	VSS_87	AG9
BD42	VSS_14	VSS_88	AH2
BD43	VSS_15	VSS_89	AH37
BD45	VSS_16	VSS_90	AH45
BD49	VSS_17	VSS_91	AH49
BD5	VSS_18	VSS_92	AJ2
BD6	VSS_19	VSS_93	AJ3
BD7	VSS_20	VSS_94	A34
BE1	VSS_21	VSS_95	AK37
BE2	VSS_22	VSS_96	AL2
BF3	VSS_23	VSS_97	AL45
A49	VSS_24	VSS_98	AL47
BF45	VSS_25	VSS_99	AL6
BF47	VSS_26	VSS_100	AM2
BF7	VSS_27	VSS_101	AM37
BG3	VSS_28	VSS_102	AN2
BG41	VSS_29	VSS_103	AN38
BG7	VSS_30	VSS_104	AN39
BH37	VSS_31	VSS_105	A36
BJ1	VSS_32	VSS_106	AN41
BJ2	VSS_33	VSS_107	AN42
BJ3	VSS_34	VSS_108	AN43
AA45	VSS_35	VSS_109	AN45
BJ41	VSS_36	VSS_110	AN49
BJ43	VSS_37	VSS_111	AN6
BJ45	VSS_38	VSS_112	AR1
BJ49	VSS_39	VSS_113	AR11
BJ7	VSS_40	VSS_114	AR2
BM11	VSS_41	VSS_115	AR3
BM3	VSS_42	VSS_116	A39
BM45	VSS_43	VSS_117	AR7
BM47	VSS_44	VSS_118	AR9
BM5	VSS_45	VSS_119	AT3
AA47	VSS_46	VSS_120	AT45
BM6	VSS_47	VSS_121	AT47
BM7	VSS_48	VSS_122	AT5
BP1	VSS_49	VSS_123	AT6
BP2	VSS_50	VSS_124	AT7
BP3	VSS_51	VSS_125	AU37
BP43	VSS_52	VSS_126	AV11
BP7	VSS_53	VSS_127	A42
BR45	VSS_54	VSS_128	AV3
BR49	VSS_55	VSS_129	AV38
AB11	VSS_56	VSS_130	AV39
AB3	VSS_57	VSS_131	AV41
AB38	VSS_58	VSS_132	AV42
AB39	VSS_59	VSS_133	AV43
AB41	VSS_60	VSS_134	AV45
A17	VSS_61	VSS_135	AV49
AB42	VSS_62	VSS_136	AV7
AB43	VSS_63	VSS_137	AY3
AB5	VSS_64	VSS_138	A44
AB6	VSS_65	VSS_139	AY7
AC45	VSS_66	VSS_140	B17
AC49	VSS_67	VSS_141	B2
AD10	VSS_68	VSS_142	B21
AD11	VSS_69	VSS_143	B24
AD34	VSS_70	VSS_144	B3
AD37	VSS_71	VSS_145	B31
A3	VSS_72	VSS_146	B48
AE6	VSS_73	VSS_147	BA1
AF37	VSS_74	VSS_148	BA2

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GND 2 OF 3

BT3	VSS_149	VSS_223	CR37
BT39	VSS_150	VSS_224	CR45
BT41	VSS_151	VSS_225	CR49
BT42	VSS_152	VSS_226	CT37
BT43	VSS_153	VSS_227	CT39
BT7	VSS_154	VSS_228	CT42
BU45	VSS_155	VSS_229	CT9
BU47	VSS_156	VSS_230	CU45
BV1	VSS_157	VSS_231	CU47
BV11	VSS_158	VSS_232	CU49
BV2	VSS_159	VSS_233	CV3
BV3	VSS_160	VSS_234	CV34
BV7	VSS_161	VSS_235	CV35
BW3	VSS_162	VSS_236	CV5
BW37	VSS_163	VSS_237	CV9
BW5	VSS_164	VSS_238	CY41
BW6	VSS_165	VSS_239	CY45
BW7	VSS_166	VSS_240	CY49
BY37	VSS_167	VSS_241	CY9
BY45	VSS_168	VSS_242	D13
BY49	VSS_169	VSS_243	D17
C11	VSS_170	VSS_244	D31
C13	VSS_171	VSS_245	D44
C14	VSS_172	VSS_246	D49
C17	VSS_173	VSS_247	DA10
C21	VSS_174	VSS_248	DA33
C24	VSS_175	VSS_249	DA9
C31	VSS_176	VSS_250	DB32
C34	VSS_177	VSS_251	DB35
C39	VSS_178	VSS_252	DB38
C48	VSS_179	VSS_253	DB45
C49	VSS_180	VSS_254	DB47
C6	VSS_181	VSS_255	DB49
CA3	VSS_182	VSS_256	DC3
CA38	VSS_183	VSS_257	DC49
CA41	VSS_184	VSS_258	DC5
CA42	VSS_185	VSS_259	DC6
CA43	VSS_186	VSS_260	DD37
CA7	VSS_187	VSS_261	DD42
CB37	VSS_188	VSS_262	DE10
CB45	VSS_189	VSS_263	DE13
CB47	VSS_190	VSS_264	DE17
CC3	VSS_191	VSS_265	DE18
CC7	VSS_192	VSS_266	DE20
CE37	VSS_193	VSS_267	DE22
CE45	VSS_194	VSS_268	DE23
CE49	VSS_195	VSS_269	DE26
CE9	VSS_196	VSS_270	DE28
CG37	VSS_197	VSS_271	DE29
CG39	VSS_198	VSS_272	DE33
CG43	VSS_199	VSS_273	DE45
CG45	VSS_200	VSS_274	DE6
CG47	VSS_201	VSS_275	DF13
CG9	VSS_202	VSS_276	DF22
CH3	VSS_203	VSS_277	DF28
CH5	VSS_204	VSS_278	DF33
CJ37	VSS_205	VSS_279	DF35
CJ42	VSS_206	VSS_280	DF39
CJ9	VSS_207	VSS_281	DG10
CK45	VSS_208	VSS_282	DG12
CK49	VSS_209	VSS_283	DG13
CK9	VSS_210	VSS_284	DG15
CL37	VSS_211	VSS_285	DG22
CL42	VSS_212	VSS_286	DG23
CL49	VSS_213	VSS_287	DG47
CM45	VSS_214	VSS_288	DG6
CM47	VSS_215	VSS_289	DH1
CM9	VSS_216	VSS_290	DH3
CN3	VSS_217	VSS_291	DH45
CN37	VSS_218	VSS_292	DH5
CN39	VSS_219	VSS_293	DJ19
CN5	VSS_220	VSS_294	DJ21
CP9	VSS_221	VSS_295	DJ27
CR32	VSS_222	VSS_296	DJ31

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DJ33	VSS_297	VSS_362	F11
DJ36	VSS_298	VSS_363	F31
DJ42	VSS_299	VSS_364	F45
DK3	VSS_300	VSS_365	F47
DK4	VSS_301	VSS_366	F8
DK49	VSS_302	VSS_367	G21
DK6	VSS_303	VSS_368	G24
DK8	VSS_304	VSS_369	G3
DL10	VSS_305	VSS_370	G31
DL13	VSS_306	VSS_371	G36
DL44	VSS_307	VSS_372	G49
DL47	VSS_308	VSS_373	G5
DM47	VSS_309	VSS_374	H17
DN15	VSS_310	VSS_375	H21
DN19	VSS_311	VSS_376	H24
DN24	VSS_312	VSS_377	H31
DN31	VSS_313	VSS_378	H33
DN36	VSS_314	VSS_379	H36
DN42	VSS_315	VSS_380	H45
DP45	VSS_316	VSS_381	H49
DR49	VSS_317	VSS_382	J10
DT1	VSS_318	VSS_383	J13
DT10	VSS_319	VSS_384	J16
DT15	VSS_320	VSS_385	J36
DT20	VSS_321	VSS_386	J6
DT27	VSS_322	VSS_387	K11
DT3	VSS_323	VSS_388	K33
DT32	VSS_324	VSS_389	K8
DT37	VSS_325	VSS_390	L36
DT42	VSS_326	VSS_391	L39
DT49	VSS_327	VSS_392	L41
DT6	VSS_328	VSS_393	L42
DT7	VSS_329	VSS_394	L43
DT8	VSS_330	VSS_395	L45
DU1	VSS_331	VSS_396	L47
DU10	VSS_332	VSS_397	M10
DU15	VSS_333	VSS_398	M3
DU2	VSS_334	VSS_399	M36
DU20	VSS_335	VSS_400	M5
DU27	VSS_336	VSS_401	N45
DU32	VSS_337	VSS_402	N49
DU37	VSS_338	VSS_403	P11
DU48	VSS_339	VSS_404	P41
DU49	VSS_340	VSS_405	P8
DU7	VSS_341	VSS_406	R3
DV2	VSS_342	VSS_407	R37
DV44	VSS_343	VSS_408	T11
DV48	VSS_344	VSS_409	T36
DV8	VSS_345	VSS_410	T41
DW1	VSS_346	VSS_411	T43
DW10	VSS_347	VSS_412	T45
DW2	VSS_348	VSS_413	T47
DW20	VSS_349	VSS_414	U3
DW27	VSS_350	VSS_415	U37
DW44	VSS_351	VSS_416	U5
DW46	VSS_352	VSS_417	V11
DW48	VSS_353	VSS_418	V36
DW49	VSS_354	VSS_419	V45
DW7	VSS_355	VSS_420	V49
E11	VSS_356	VSS_421	V9
E34	VSS_357	VSS_422	W37
E36	VSS_358	VSS_423	Y36
E39	VSS_359	VSS_424	Y38
E42	VSS_360	VSS_425	Y43
E6	VSS_361	VSS_426	Y9
		VSS_427	DE15

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Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P017 - ICL-U(12/13)GND**

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

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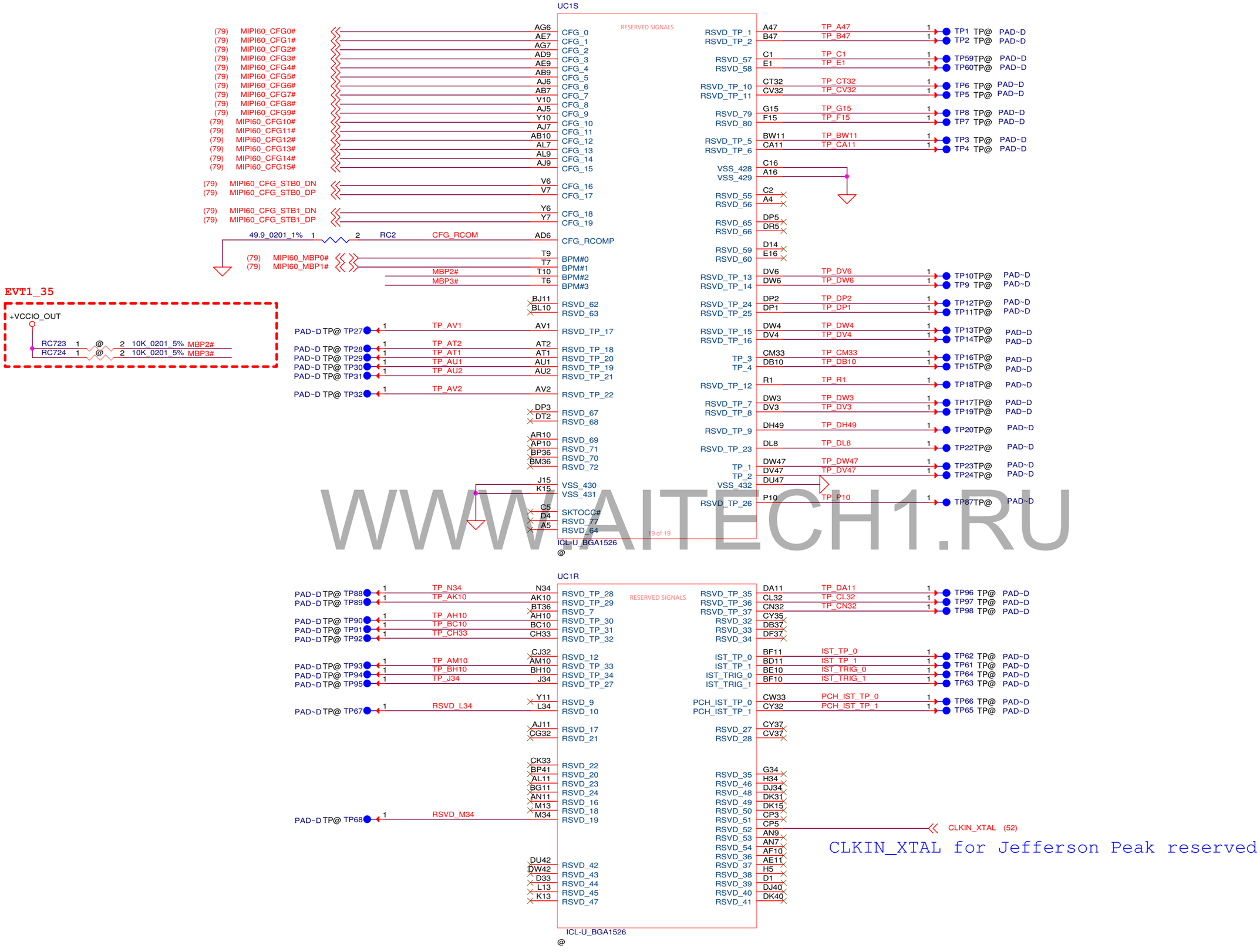

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P018 - ICL-U(13/13)RSVD,MIPI60
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
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Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title	***P019 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 19 of 101	

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: ***P020 - Reserve***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 20 of 101	

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

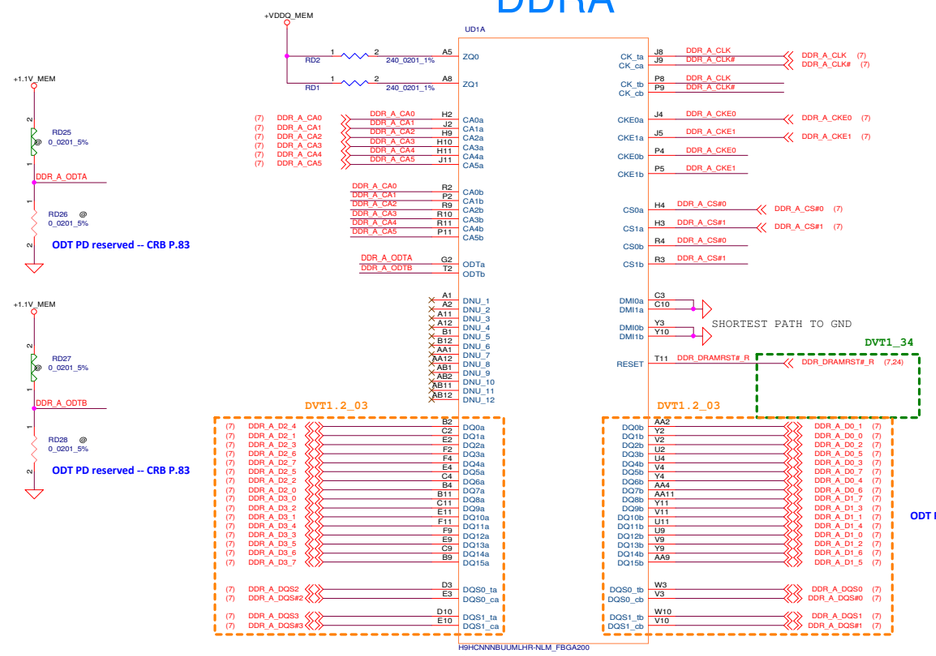
Compal Electronics, Inc.		
Title: ***P021 - Reserve***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 21 of 101	

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

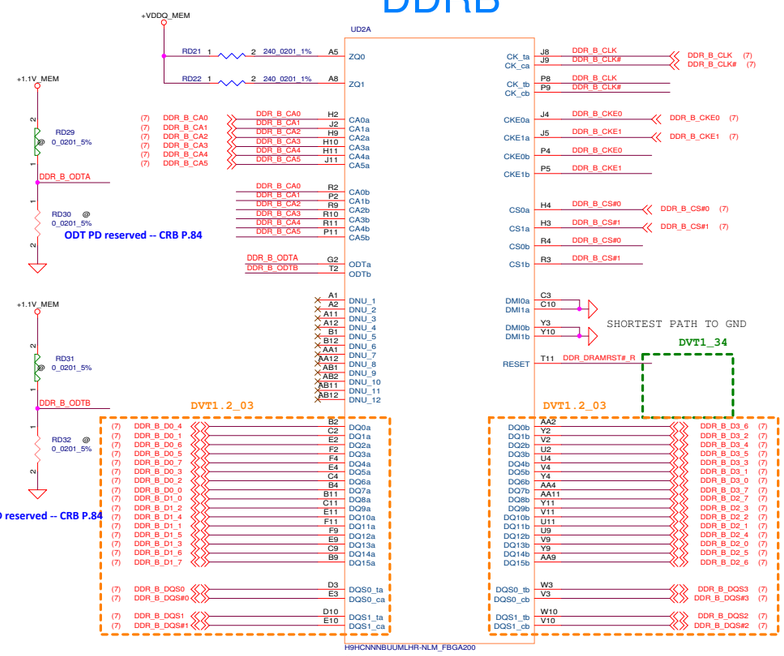
Compal Electronics, Inc.		
Title	***P022 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 22 of 101	

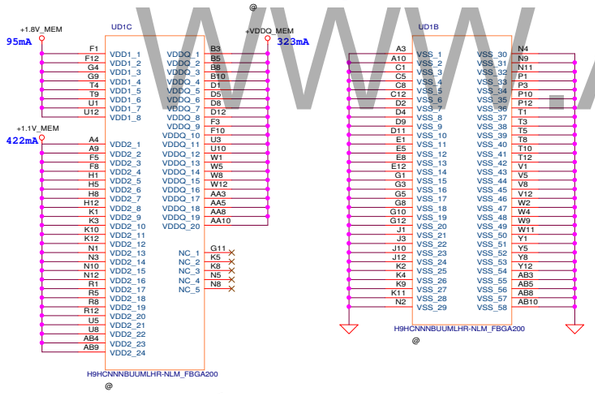
Memory connection follow J72913-201 Rev 01_20181217

DDRA

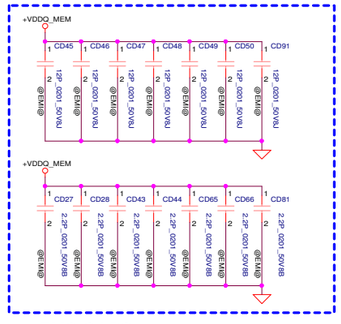


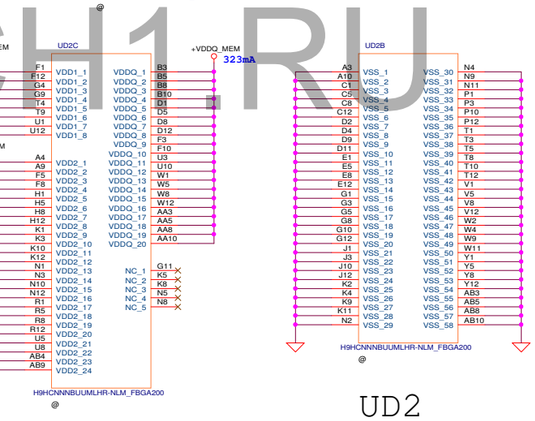
DDRB



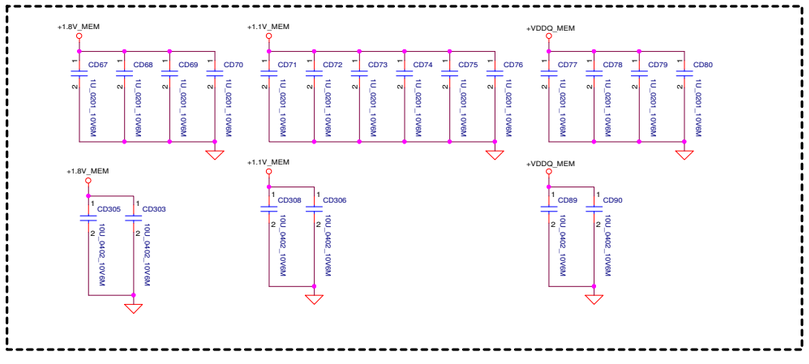


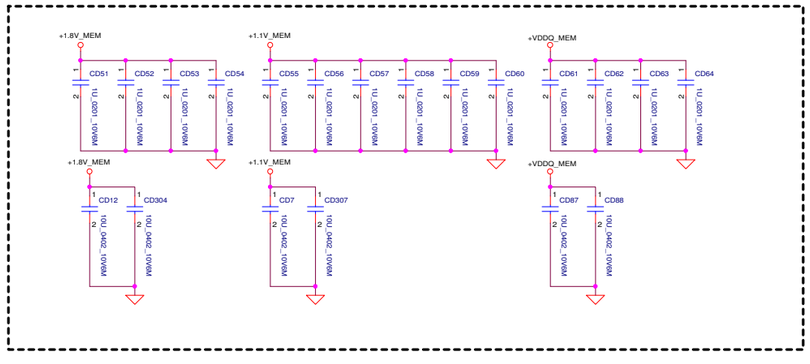
UD1





UD2





Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P023 - LPDDR4/x Channel A/B		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
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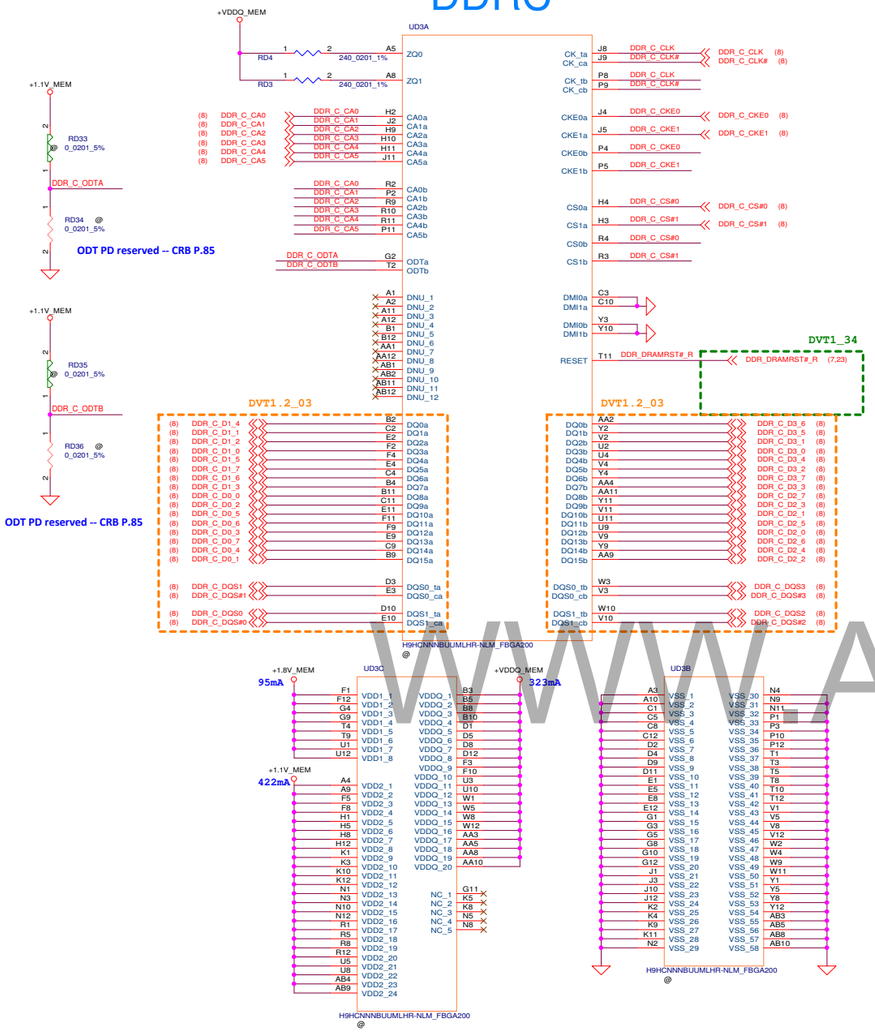
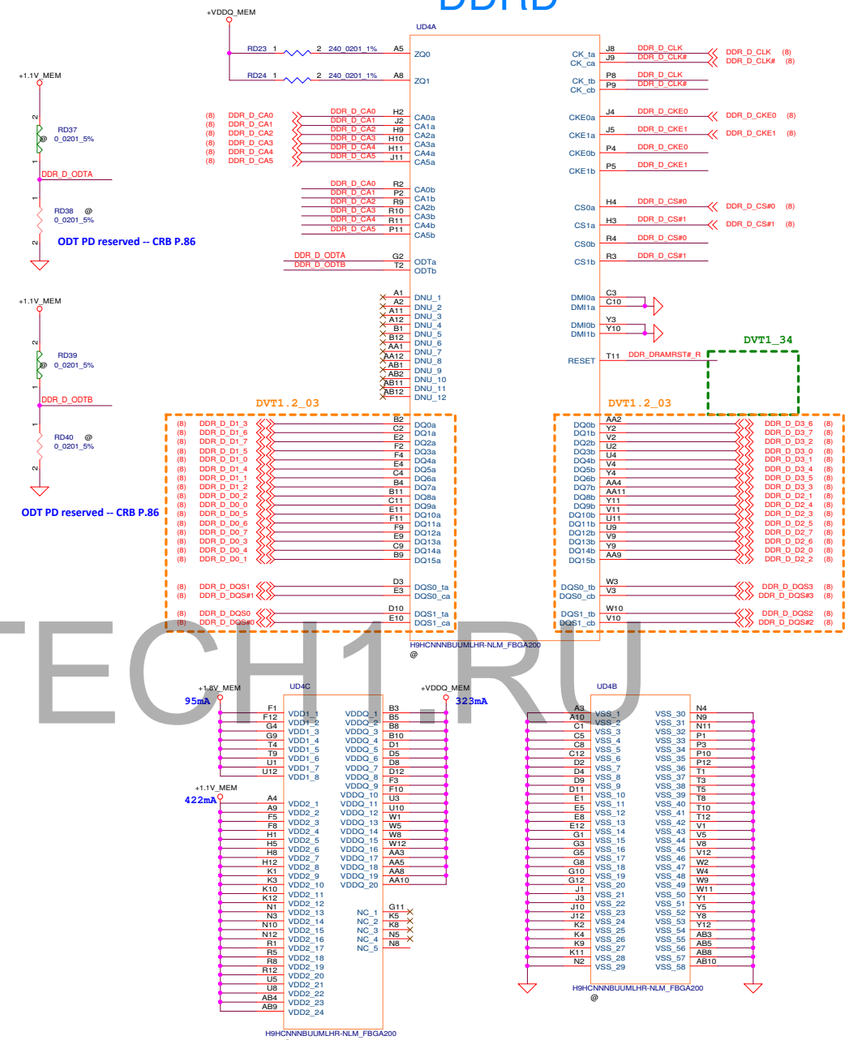
Memory connection follow J72913-201 Rev 01_20181217

DDRC

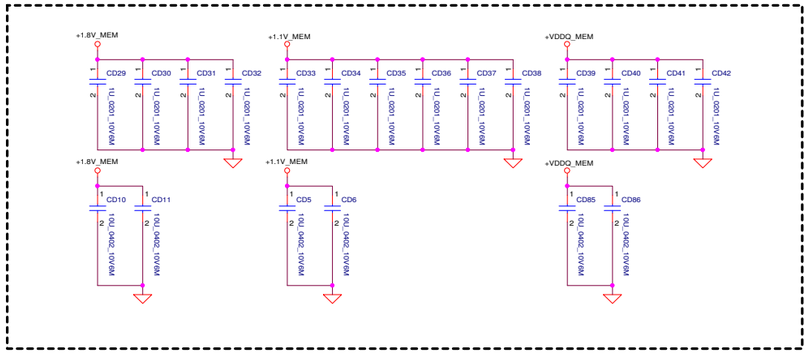


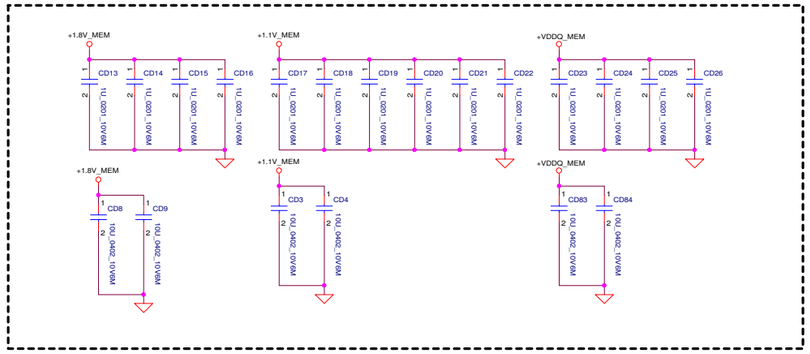
DDRD



UD3

UD4





Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P024 - LPDDR4/x Channel C/D
Size	Document Number: LA-G172P
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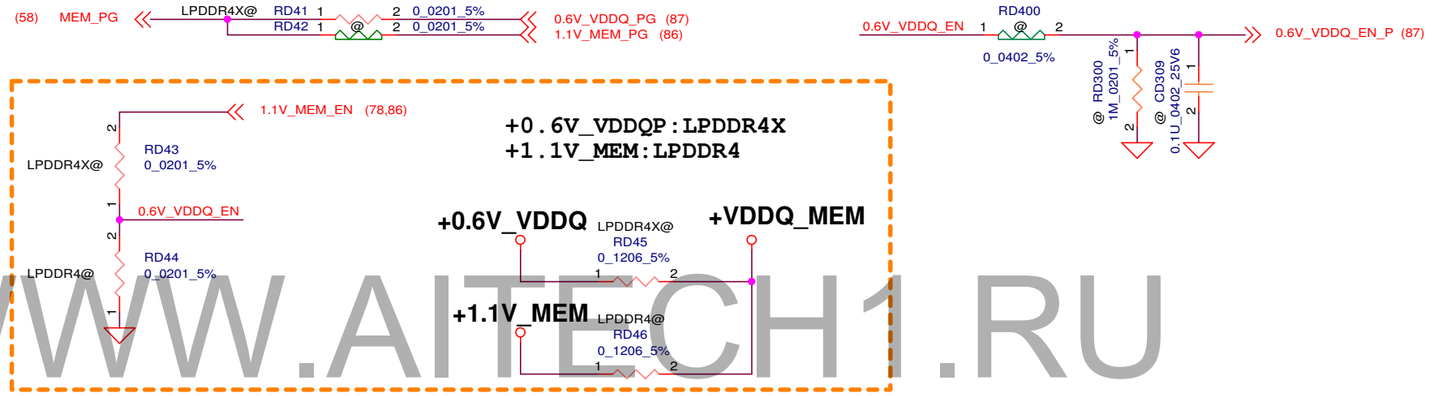

	RD43	RD45	RD44	RD46
LPDDR4(1.1V) :	@	@		
LPDDR4X(1.1v&0.6V):			@	@

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28
Title	P025 - LPDDR4&4X BOM OPTION		
Size	Document Number LA-G172P		Rev 1.0 (A00)
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Compal Electronics, Inc.

Title: **P026 - Reserve**

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Compal Electronics, Inc.		
Title	***P027 - Reserve***	
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Compal Electronics, Inc.		
Title	***P028 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 28 of 101	

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Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: ***P029 - Reserve***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
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Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title	***P030 - Reserve***	
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Compal Electronics, Inc.		
Title: ***P031 - Reserve***		
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Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: ***P032 - Reserve***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
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Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title	***P033 - Reserve***	
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Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: ***P034 - Reserve***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
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Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: ***P035 - Reserve***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title	***P036 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
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Compal Electronics, Inc.		
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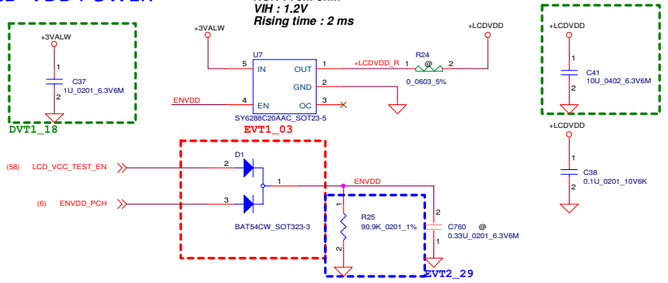
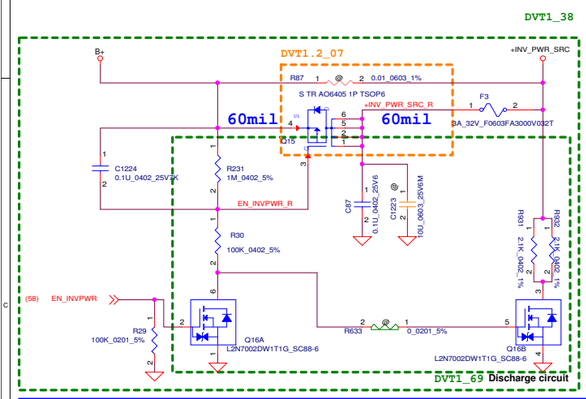
LCD VDD POWER

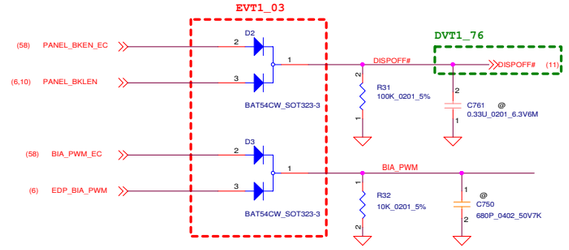
OCP : 1.5A
RON : 70m ohm
VIH : 1.2V
Rising time : 2 ms



eDP BackLight Power



BackLight PWM Control



eDP Conn

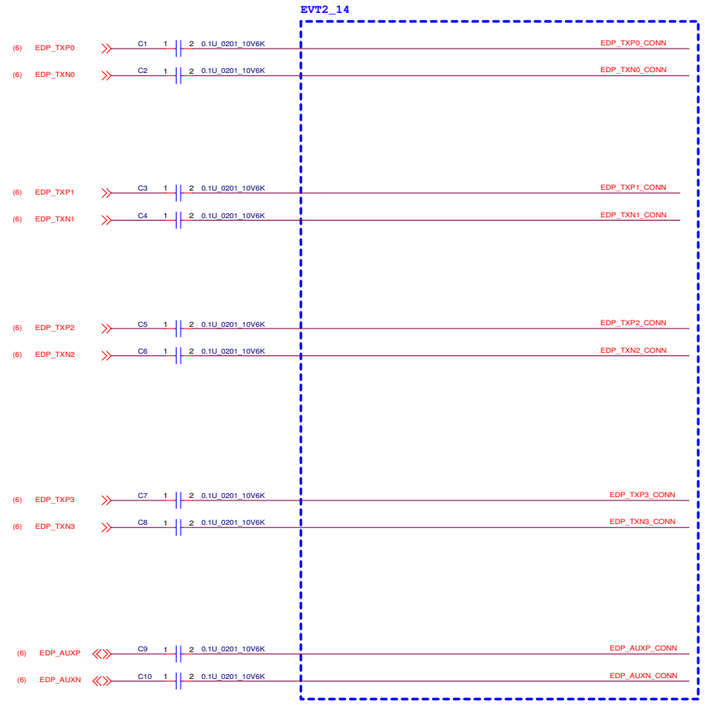
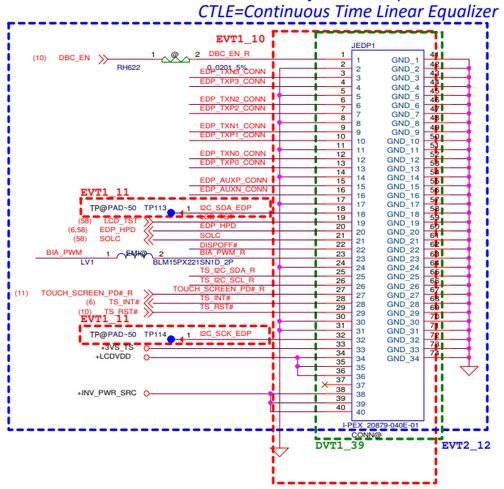
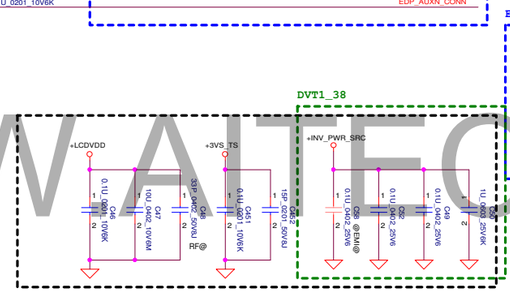


Table 5-41. eDP* Bit Rates

Bit Rate	Lane Supports (max # of lanes)	Peak Bandwidth
1.62 Gb/s (RBR)	4	4 x 162 MB/s = 648 MB/s
2.7 Gb/s (HBR)	4	4 x 270 MB/s = 1080 MB/s
5.4 Gb/s (HBR2)	4	4 x 540 MB/s = 2160 MB/s
8.1 Gb/s (HBR3)	4	4 x 810 MB/s = 3240 MB/s

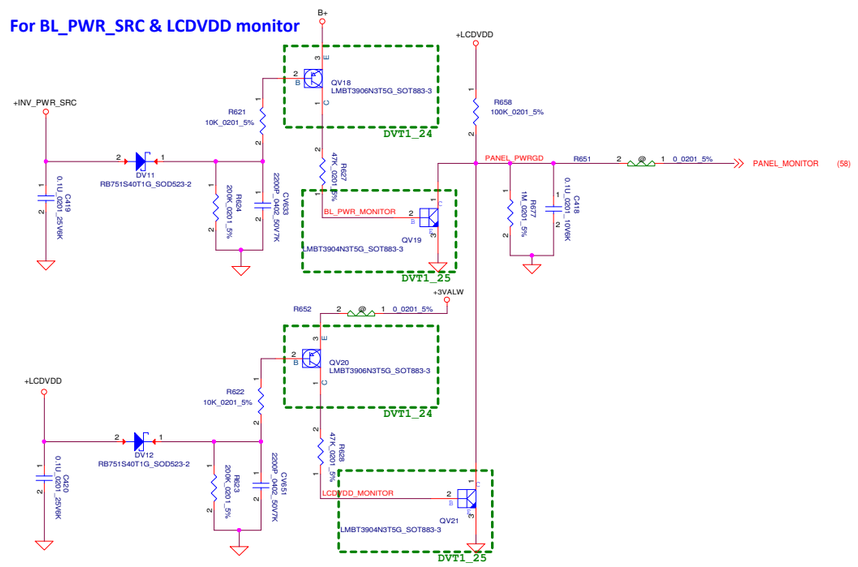
eDP Bit Rates 8.1 Gb/s (HBR3)*
In TCON side , RX Equalization is CTLE + DFE
DFE=Decision feedback equalizer
CTLE=Continuous Time Linear Equalizer

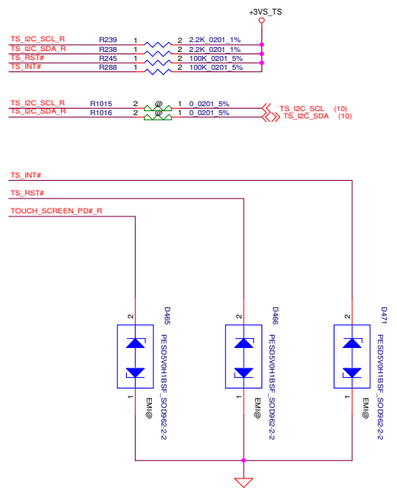




Connecter	Pin	NAME	IN/OUT	FUNCTION
CN1	1	/STOP	I	HIGH : Normal Operation LOW : Stop Scanning Build-in pull/up (to 3.3 volts) resistor 35kohm
	2	IIC SDA	I/O	IIC Data Open drain output, pull-up resister at Host is needed
	3	IIC SCL	I	IIC Clock Open drain output, pull-up resister at Host is needed
	4	NC	-	No Connection
	5	NC	-	No Connection
	6	IIC IRQ	O	IIC Data Ready Output "LOW" when data ready to send Open drain output, pull-up resister at Host is needed
	7	/RESET	I	Hardware RESET : Low Active Stop operation when pull "LOW" Build-in pull-up (to 3.3 volts) resister 100kohm
	8	VDD +3.3V	-	3.3 volts (typ) power input
	9	NC	-	No Connection
	10	DGND	-	Ground

For BL_PWR_SRC & LCDVDD monitor





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	P038 - eDP,Touch Screen
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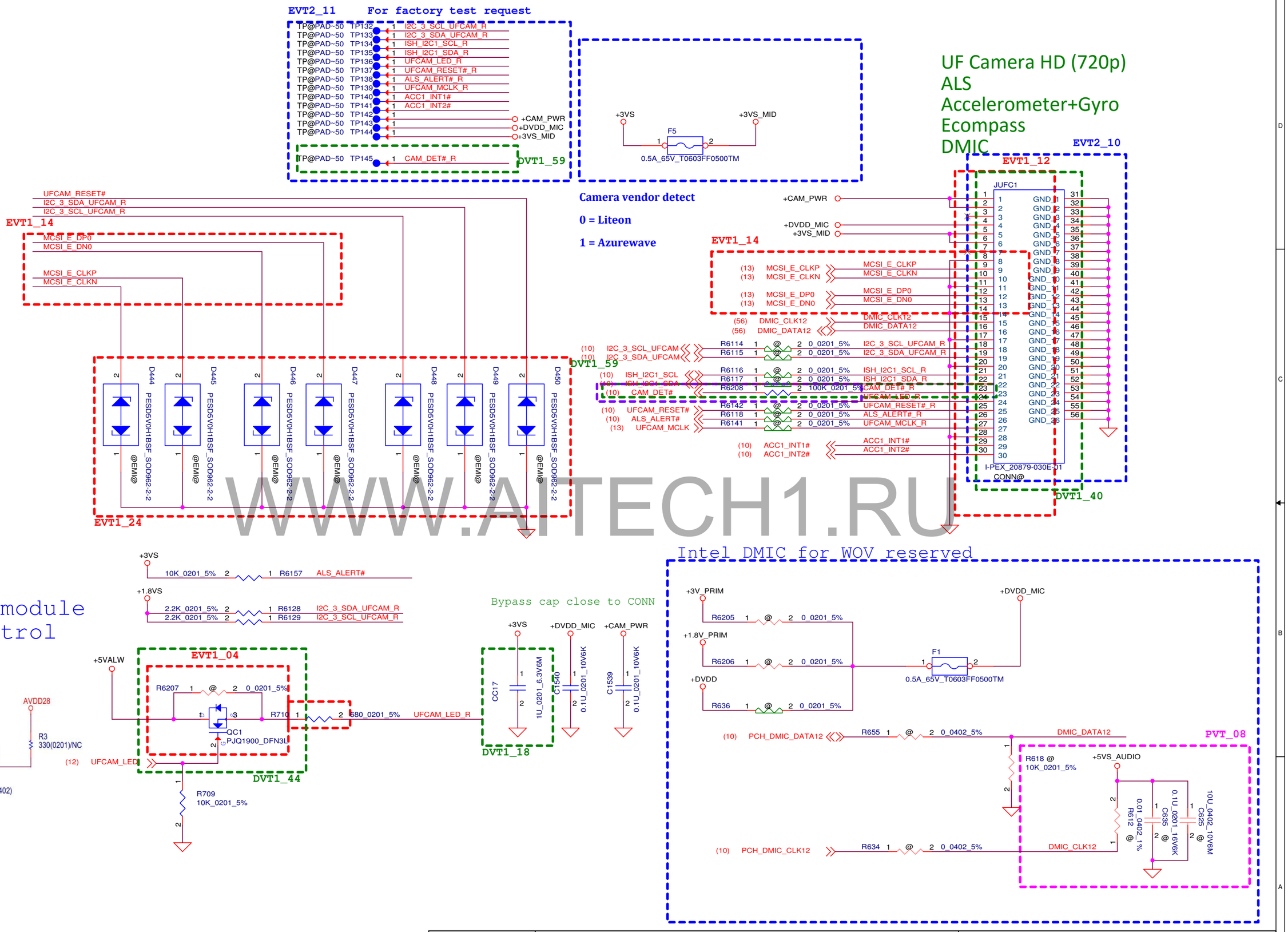

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P039 - UF Camera,MIC,ALS			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
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Compal Electronics, Inc.		
Title	***P040 - Reserve***	
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Compal Electronics, Inc.		
Title	***P041 - Reserve***	
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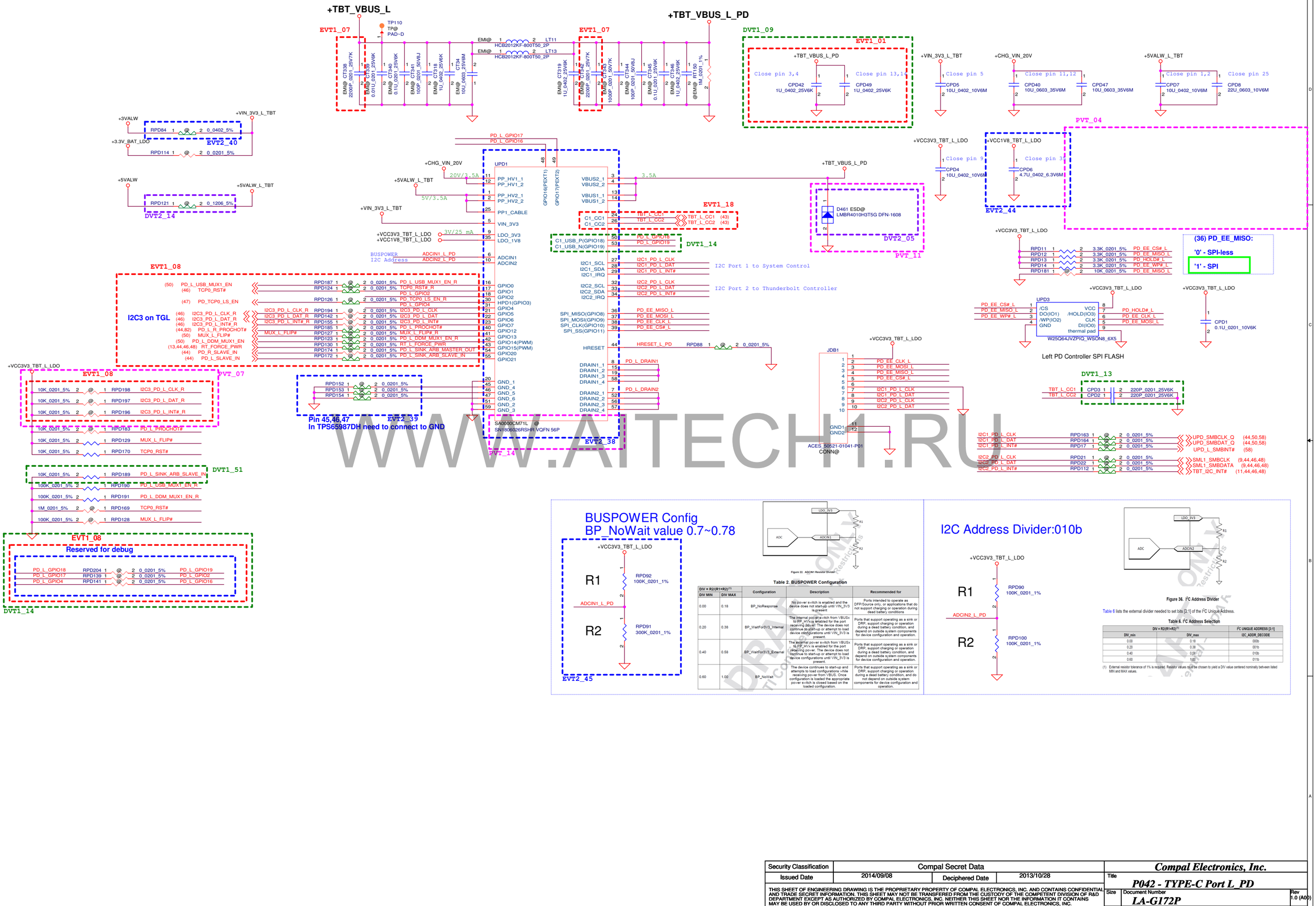

BUSPOWER Config
BP_NoWait value 0.7~0.78

Figure 22. ADCIN1 Resistor Divider

Table 2. BUSPOWER Configuration

DIV = R2/(R1+R2)(1)		Configuration	Description	Recommended for
DIV MIN	DIV MAX			
0.00	0.18	BP_NoResponse	No power switch is enabled and the device does not start-up until VIN_3V3 is present	Ports intended to operate as DFP/Source only, or applications that do not support charging or operation during dead battery conditions
0.20	0.38	BP_WaitForV3V3_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.40	0.58	BP_WaitForV3V3_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.60	1.00	BP_NoWait	The device continues to start-up and attempts to load configurations while receiving power from VBUS. Once configuration is loaded the appropriate power switch is closed based on the loaded configuration.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and do not depend on outside system components for device configuration and operation.

I2C Address Divider:010b

Figure 36. I²C Address Divider

Table 6 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 6. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]
DIV_min	DIV_max	I2C_ADDR_DECODE
0.00	0.18	000b
0.20	0.38	001b
0.40	0.58	010b
0.60	1.00	011b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

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Title	P042 - TYPE-C Port L_PD		
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LEFT Type-C Connector

EVT2_08

(46) TBT_0_TTX_CD_DRX_P0
(46) TBT_0_TTX_CD_DRX_N0
CT30 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_P0
CT31 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_N0

(46) TBT_0_TTX_CD_DRX_P1
(46) TBT_0_TTX_CD_DRX_N1
CT32 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_P1
CT33 1 2 0.22U_0201_6.3V6M TBT_0_TTX_C_DRX_N1

EVT1_05

DVT1_02
EVT2_22

+TBT_VBUS_L
JUSBC1
TBT_0_TTX_C_DRX_P0
TBT_0_TTX_C_DRX_N0
CT3101 2 0.1U_0201_25V6K
(42) TBT_L_CC1
SW_TBT_L_USB20_P1_R
SW_TBT_L_USB20_N1_R
(46) TBT_0_SBU1
CT3121 2 0.1U_0201_25V6K
(46) TBT_0_TRX_RT_DTX_N1
(46) TBT_0_TRX_RT_DTX_P1
JUSBC1_GND
A1 GND_1
A2 SSTXp1
A3 SSTXn1
A4 VBUS_1
A5 CC1
A6 Dp1
A7 Dn1
A8 SBU1
A9 VBUS_2
A10 SSRXn2
A11 SSRXp2
A12 GND_2
1 GND_5
2 GND_7
3 GND_9
4 GND_11
TOP
BOTTOM
GND_4 B12
SSRXp1 B11
SSRXn1 B10
VBUS_4 B9
SBU2 B8
Dn2 B7
Dp2 B6
CC2 B5
VBUS_3 B4
SSTXn2 B3
SSTXp2 B2
GND_3 B1
5 GND_6
6 GND_8
7 GND_10
8 GND_12
FOX_UT12123-10001-7H CONN@

+TBT_VBUS_L
CT347 10U_0603_25V6M

EVT2_08
TBT_0_TRX_RT_DTX_P0 (46)
TBT_0_TRX_RT_DTX_N0 (46)
2 CT1313 0.1U_0201_25V6K
TBT_0_SBU2
TBT_0_SBU2 (46)
SW_TBT_L_USB20_N2_R
SW_TBT_L_USB20_P2_R
TBT_L_CC2
TBT_L_CC2 (42)
2 CT1311 0.1U_0201_25V6K
TBT_0_TTX_C_DRX_N1
TBT_0_TTX_C_DRX_P1
EVT1_18

+TBT_VBUS_L
AZ4520-01F.R7G_DFN1610P2E2
D459 ESD@
DVT1_23

EVT1_26
EVT2_08

JUSBC1_GND
LT1 EMI@ HCB2012KF-800T50_2P
EMI@ CT35 0.1U_0201_25V6K

EVT1_18
TBT_0_SBU1
TBT_0_SBU2
@ CT206 100P_0201_50V8J
RT118 @ 1M_0201_1%
@ CT207 100P_0201_50V8J
RT119 @ 1M_0201_1%

EVT2_08

PVT_05

ML6 EMI@
(50) SW_TBT_L_USB20_N1
(50) SW_TBT_L_USB20_P1
SW_TBT_L_USB20_N1_R
SW_TBT_L_USB20_P1_R
HCM1012GH900BP_4P

ML7 EMI@
(50) SW_TBT_L_USB20_N2
(50) SW_TBT_L_USB20_P2
SW_TBT_L_USB20_N2_R
SW_TBT_L_USB20_P2_R
HCM1012GH900BP_4P

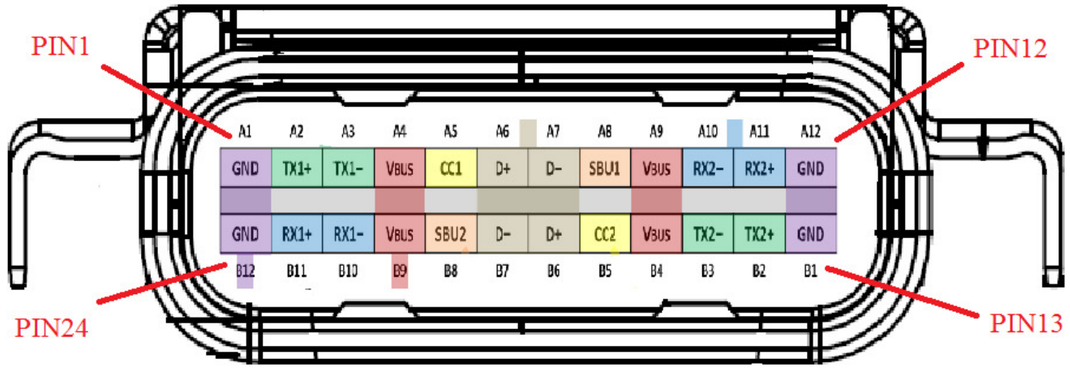
EVT2_08

D75 ESD@ TBT_0_TTX_C_DRX_P0
D76 ESD@ TBT_0_TTX_C_DRX_P1
D77 ESD@ TBT_0_TTX_C_DRX_N0
D78 ESD@ TBT_0_TTX_C_DRX_N1
D79 ESD@ TBT_0_TRX_RT_DTX_P0
D80 ESD@ TBT_0_TRX_RT_DTX_P1
D81 ESD@ TBT_0_TRX_RT_DTX_N0
D82 ESD@ TBT_0_TRX_RT_DTX_N1
PESD5V0H1BSF_SOD962-2-2

ESD Diodes should be located as close as possible to USBC.

D407 ESD@ SW_TBT_L_USB20_P1_R1
D408 ESD@ SW_TBT_L_USB20_N1_R
D409 ESD@ SW_TBT_L_USB20_P2_R1
D410 ESD@ SW_TBT_L_USB20_N2_R
D411 ESD@ TBT_L_CC1
D412 ESD@ TBT_0_SBU1
D413 ESD@ TBT_0_SBU2
D414 ESD@ TBT_L_CC2
PESD5V0H1BSF_SOD962-2-2

EVT1_18



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P043 - TYPE-C Conn L
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+TBT_VBUS_R

+TBT_VBUS_R_PD

I2C3 on TGL

I2C Port 1 to System Control

I2C Port 2 to Thunderbolt Controller

Right PD Controller SPI FLASH

Pin 45,46,47 In TPS65987DH need to connect to GND

Reserved for debug

BUSPOWER Config
BP_NoWait value 0.7~0.78

I2C Address Divider:000b

Table 2. BUSPOWER Configuration

DIV = R2/(R1+R2)(1)		Configuration	Description	Recommended for
DIV MIN	DIV MAX			
0.00	0.18	BP_NoResponse	No power switch is enabled and the device does not start-up until VIN_3V3 is present.	Ports intended to operate as DFP/Source only, or applications that do not support charging or operation during dead battery conditions
0.20	0.38	BP_WaitFor3V3_Internal	The internal power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.40	0.58	BP_WaitFor3V3_External	The external power switch from VBUSx to PP_HVx is enabled for the port receiving power. The device does not continue to start-up or attempt to load device configurations until VIN_3V3 is present.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and depend on outside system components for device configuration and operation.
0.60	1.00	BP_NoWait	The device continues to start-up and attempts to load configurations while receiving power from VBUS. Once configuration is loaded the appropriate power switch is closed based on the loaded configuration.	Ports that support operating as a sink or DRP, support charging or operation during a dead battery condition, and do not depend on outside system components for device configuration and operation.

Figure 36. I²C Address Divider

Table 6 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 6. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]
DIV_min	DIV_max	I2C_ADDR_DECODE
0.00	0.18	000b
0.20	0.38	001b
0.40	0.58	010b
0.60	1.00	011b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P044 - TYPE-C Port R_PD
Size	Document Number: LA-G172P
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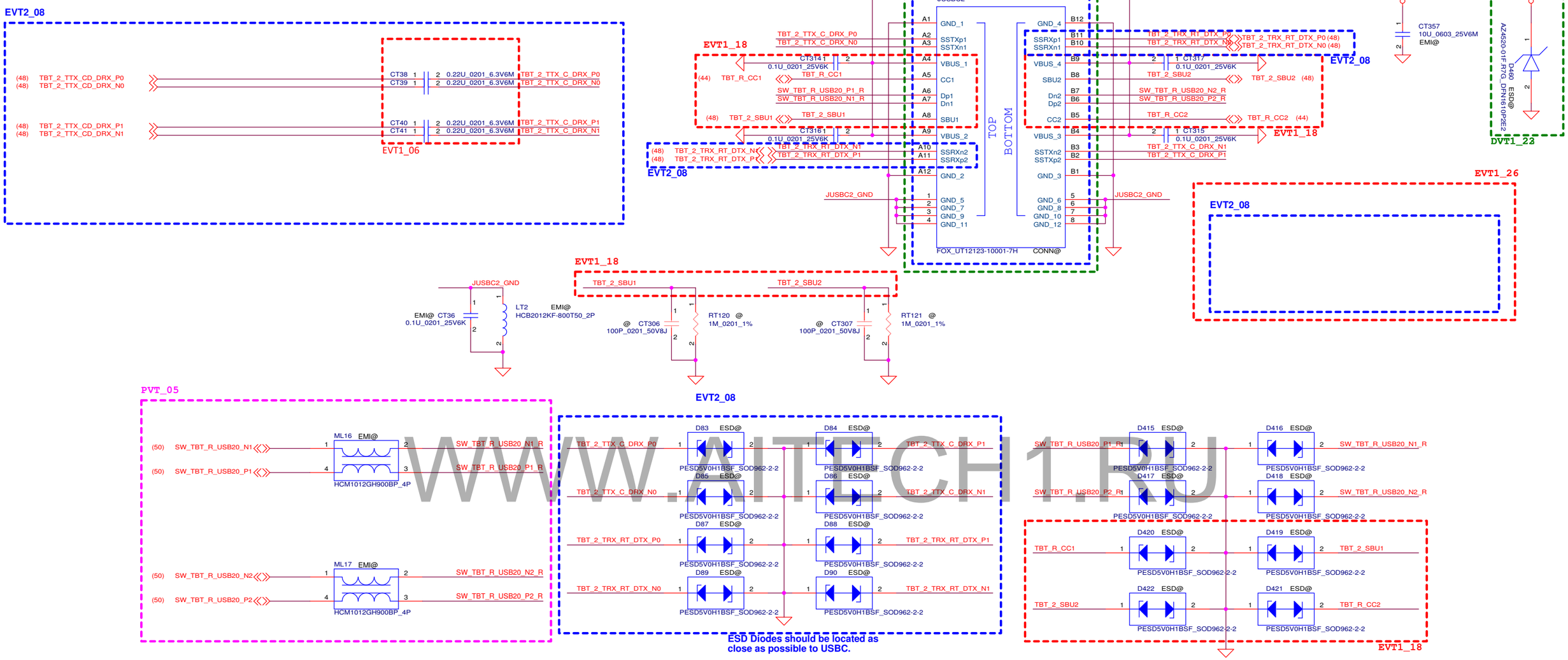
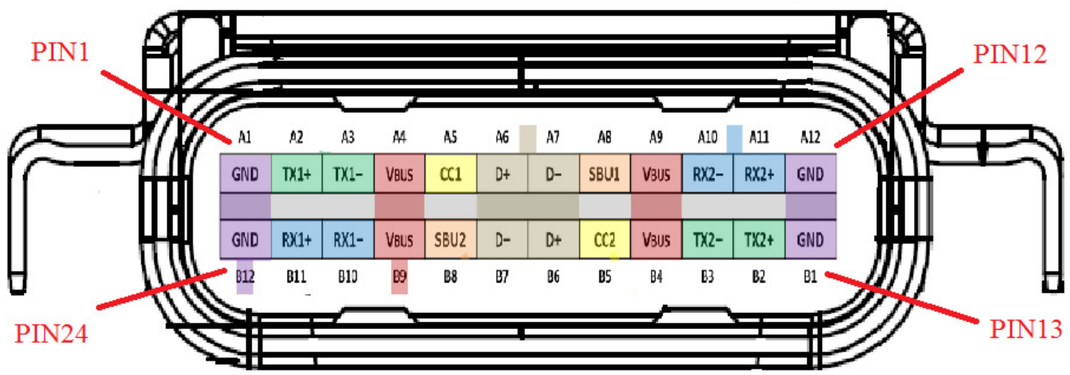
RIGHT Type-C Connector





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date 2013/10/28	Title: P045 - TYPE-C Conn R
			Size: Document Number: LA-G172P Rev: 1.0 (A00)
			Date: Friday, May 24, 2019 Sheet 45 of 101

TBT PORTS

URT1D @

BURNSIDE-BRIDGE_BGA105

Port A - Host Side

Port B - TypeC Side

EVT2_08

EVT1_18

MISC & DEBUG

URT1A @

BURNSIDE-BRIDGE_BGA105

Follow CSLP

Intel suggestion

A12:
DB connect to GND.
BB is NC.

B3 PD 100 ohm

A1,A2 SDS,CRB is NC

POC_GPIO_12 have iPU

DVT1_66

PVT_14

EVT1_10

PD I2C3 on TGL

PCH

SMBUS:
No support Vpro
Intel recommended PD 100K

DVT1_47

Reserve for TBT RTD3 Support

RT ref p.5 XTAL Recommended
FW2500025Z by Pericom
XRCGB25M000F3L12R0 by Murata

Suggest adding GND shield across
Crystal and 18pF caps for better
RFI.

DVT1_35

EVT1_37

PVT_09

PVT_04

EVT2_26

Debug

DVT1.2_13

DVT1_49 DVT1_80

For BBR-A0 PLL Issue Workaround reserved

DVT1_49 DVT1_80

(L11) DG_P1_RST#:

For PD based systems, DG_P1_RST# should be output from PD.

For TCPC based systems, DG_P1_RST# should be output from SOC/EC.

(B10) FORCE_PWR:Connect to PCH for FW update

'0' - by default

'1' - for debug only

(A9) DG_FLASH_BUSY#:conenction to PU

(A4) DG_FLSH_SHARE_EN (iPU):

'0' - Flash isn't shared. 1 Flash per Re-timer. Can be left NC.

'1' - Flash is shared between 2 Re-timers.

(A5) DG_FLSH_MSTR_SLV (iPU):

'0' - Set Re-timer to be Slave on shared flash SPI I/F.

'1' - Set Re-timer to be Master on shared flash SPI I/F.

(A8) DG_POC_GPIO6:

'0' -Reserved for debug

'1' -Indication to S0 state for Re-timer

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P046 - TYPE-C TBT_BB L_TCSS
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
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EVT2_41
+3.3V_TBT_L_LC
CT57 1U_0201_6.3V6K
Place near Pin E5
+3.3V_TBT_L_ANA
CT58 1U_0201_6.3V6K
Place near Pin L2

+0.9V_TBT_L_LVR
EVT2_41
CT60 1U_0201_6.3V6K
CT200 10U_0402_10V6M
Place near Pin L6,M6
+0.9V_TBT_L_LC
EVT2_41
CT59 1U_0201_6.3V6K
Place near Pin J3

URT1B @
+3.3V_TBT_L_ANA → L2 VCC3P3_ANA
+3.3V_TBT_L_LC → E5 VCC3P3_LC
+0.9V_TBT_L_SVR → F6 VCC0P9_SVR_ANA_1, G6 VCC0P9_SVR_ANA_2
E3 VCC0P9_SVR_1, G3 VCC0P9_SVR_2
+0.9V_TBT_L_LC → E9 VCC0P9_SVR_PB_ANA_1, G9 VCC0P9_SVR_PB_ANA_2
+0.9V_TBT_L_LVR → J3 VCC0P9_LC, L6 VCC0P9_LVR, M6 VCC0P9_LVR_SENSE
Power
BURNSIDE-BRIDGE_BGA105

VCC3P3_SX E6 +3.3V_TBT_L_SX 1 @ 2 0_0402_5% RT180
VCC3P3_SVR_1 M4 +3.3V_TBT_L_SVR 1 @ 2 0_0402_5% RT181
VCC3P3_SVR_2 M5
VCC3P3_SVR_3 J5 +3.3V_TBT_L_DB 1 2
VCC3P3A J7 RT203 DLB@ 0_0201_5%
+3.3V_TBT_L
+3.3VA_TBT_L
SVR_IND_1 L1
SVR_IND_2 M1
+TBT_L_SVR_IND
connect via inductor to VCC0P9_SVR
SVR_VSS_1 M2
SVR_VSS_2 M3
NC_J6 J6 RT122 1 DLB@ 2 0_0201_5%

J5:
DB connect to +3.3V_TBT_L.
BB is NC.

J6:
DB connect to GND.
BB is NC.

EVT2_41
+3.3V_TBT_L_SVR
CT3365 47U_0603_6.3V6M
CT163 1U_0201_6.3V6K
CT62 1U_0201_6.3V6K
Place near Pin M4, M5, J5
GND share with Pin M2, M3
3.3v @ 290mA
+3.3V_TBT_L_SX
CT61 1U_0201_6.3V6K
Place near Pin E6
3.3v @ 80mA

+3.3V_TBT_L
RT79 1 @ 2 0_0402_5%
+3.3VA_TBT_L
EVT2_41
CT303 10U_0402_10V6M
CT302 18P_0201_25V8J
CT64 1U_0201_6.3V6K
Place near Pin J7
3.3v @ 50mA

+TBT_L_SVR_IND
LT8
0.68UH_MLV-YT10NR68N-M1L_2.7A_30%
EVT2_41
+0.9V_TBT_L_SVR
CT49 1U_0201_6.3V6K
CT50 1U_0201_6.3V6K
CT51 1U_0201_6.3V6K @
CT52 1U_0201_6.3V6K @
CT53 1U_0201_6.3V6K @
CT54 1U_0201_6.3V6K
CT55 47U_0603_6.3V6M
CT56 18P_0201_25V8J
Place near Pin F6,G6,E3,G3,E9,G9
GND share with Pin M2, M3
0.9v @ 850mA
DVT1_06
DVT1_53 BB ref sch Rev 1.4 change to CAP Place near Pin F6,E3,E9
G3,G6,G9 CAP change to NC

+3VALW
CT361 1U_0201_6.3V6K
+3VALW
UT1
VIN_1 VIN_2 VOUT_1 VOUT_2 ON CT VBIAS GND_1 GND_2
AOZ1336DI_DFN8_2X2
(42) PD_TCP0_LS_EN → RT83 1 @ 2 0_0201_5%
(11,16,49,58) SIO_SLP_SUS# → RT84 1 @ 2 0_0201_5%
3.3V_TBT_L_EN
+3.3V_TBT_L_B
LT3
EMI@
BLM18KG331SN1D_2P
3.3v @ 370mA
+3.3V_TBT_L
CT362 470P_0402_50V7K
CT363 0.1U_0201_10V6K
+3.3V_TBT_L
3.3V_TBT_L_EN RT178 1 2 100K_0201_5%
RT179 1 @ 2 10K_0201_5%
+3VALW
EVT2_34

URT1C
GND
VSS_ANA_1 B1, VSS_ANA_2 B12, VSS_ANA_3 D1, VSS_ANA_4 D2, VSS_ANA_5 D11, VSS_ANA_6 D12, VSS_ANA_7 F1, VSS_ANA_8 F2, VSS_ANA_9 F7, VSS_ANA_10 F9, VSS_ANA_11 F11
VSS_ANA_12 F12, VSS_ANA_13 G7, VSS_ANA_14 H1, VSS_ANA_15 H2, VSS_ANA_16 H11, VSS_ANA_17 H12, VSS_ANA_18 J9, VSS_ANA_19 K1, VSS_ANA_20 K2, VSS_ANA_21 K11, VSS_ANA_22 K12
VSS_1 G5, VSS_2 F5, VSS_3 F3
BURNSIDE-BRIDGE_BGA105
@

BB ref sch p.6 note
DG_P1_PWR_GATE_EN:

For PD based systems, DG_P1_PWR_GATE_EN should be output from PD.

For TCPC based systems, DG_P1_PWR_GATE_EN should be output from SOC/EC.

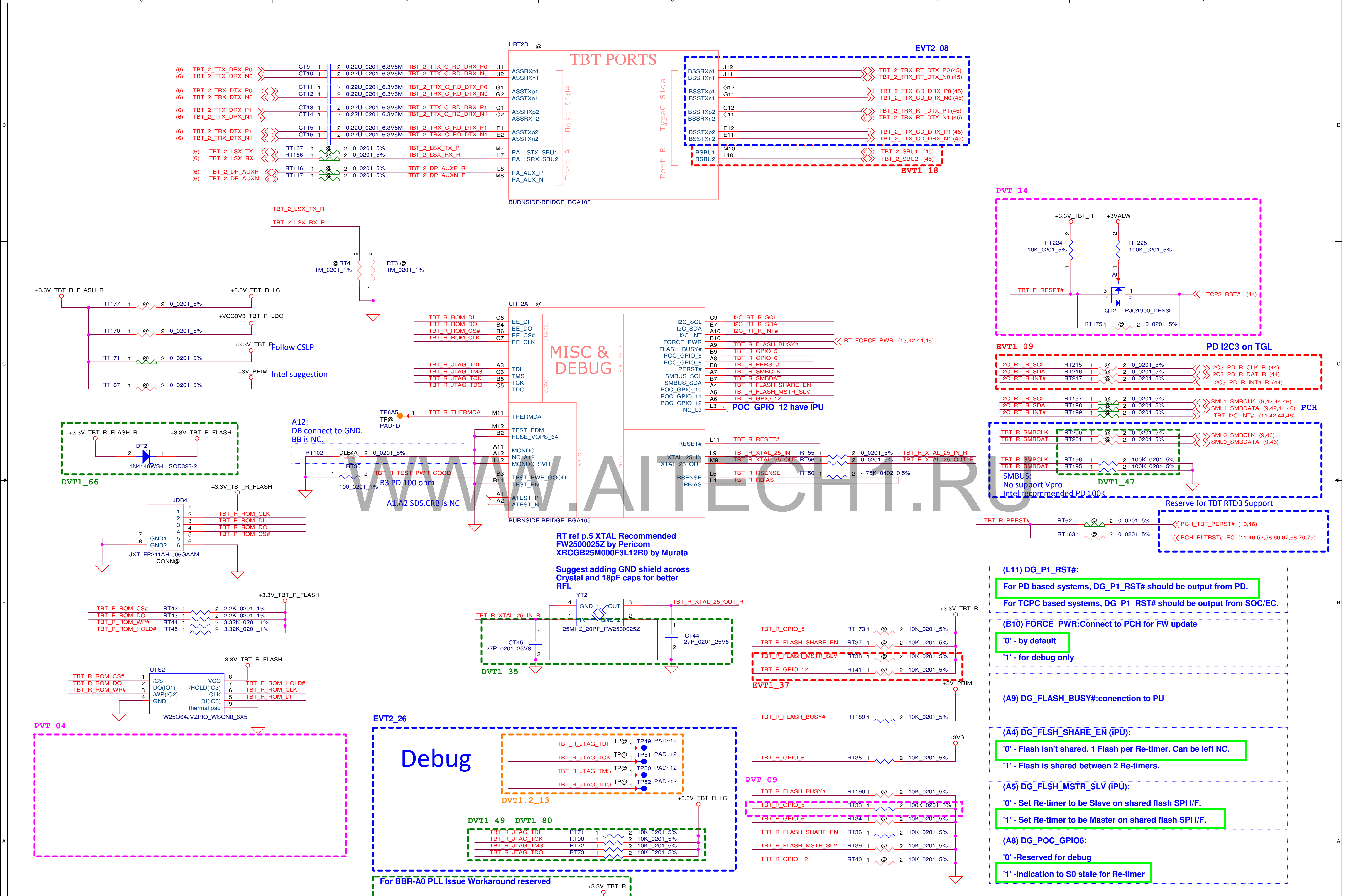
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P047 - TYPE-C TBT_BB L_PWR,GND

Size | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 47 of 101



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P048 - TYPE-C TBT_BB R_TCSS*

Size | Document Number: *LA-G172P* | Rev 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 48 of 101

EVT2_41

+3.3V_TBT_R_LC — CT68 1U_0201_6.3V6K — Place near Pin E5

+3.3V_TBT_R_ANA — CT69 1U_0201_6.3V6K — Place near Pin L2

+0.9V_TBT_R_LVR — EVT2_41 — CT84 1U_0201_6.3V6K, CT201 10U_0402_10V6M — Place near Pin L6,M6

+0.9V_TBT_R_LC — EVT2_41 — CT82 1U_0201_6.3V6K — Place near Pin J3

URT2B @ — BURNSIDE-BRIDGE_BGA105

+3.3V_TBT_R_ANA	L2	VCC3P3_ANA	
+3.3V_TBT_R_LC	E5	VCC3P3_LC	
+0.9V_TBT_R_SVR	F6	VCC0P9_SVR_ANA_1	
	G6	VCC0P9_SVR_ANA_2	
	E3	VCC0P9_SVR_1	
	G3	VCC0P9_SVR_2	
	E9	VCC0P9_SVR_PB_ANA_1	
+0.9V_TBT_R_LC	G9	VCC0P9_SVR_PB_ANA_2	
+0.9V_TBT_R_LVR	J3	VCC0P9_LC	
	L6	VCC0P9_LVR	
	M6	VCC0P9_LVR_SENSE	
		Power	
	E6	VCC3P3_SX	+3.3V_TBT_R_SX — RT184 — +3.3V_TBT_R
	M4	VCC3P3_SVR_1	+3.3V_TBT_R_SVR — RT185 — +3.3V_TBT_R
	M5	VCC3P3_SVR_2	
	J5	VCC3P3_SVR_3	+3.3V_TBT_R_DB — RT202 DLB@ 0_0201_5% — +3.3VA_TBT_R
	J7	VCC3P3A	
	L1	SVR_IND_1	+TBT_R_SVR_IND
	M1	SVR_IND_2	
	M2	SVR_VSS_1	
	M3	SVR_VSS_2	
NC_J6	J6		RT123 DLB@ 0_0201_5%

J5:
DB connect to +3.3V_TBT_R.
BB is NC.

connect via inductor to VCC0P9_SVR

J6:
DB connect to GND.
BB is NC.

EVT2_41

+3.3V_TBT_R_SVR — CT366 47U_0603_6.3V6M, CT72 1U_0201_6.3V6K, CT71 1U_0201_6.3V6K

+3.3V_TBT_R_SX — CT70 1U_0201_6.3V6K

Place near Pin M4, M5, J5
GND share with Pin M2, M3
3.3v @ 290mA

Place near Pin E6
3.3v @ 80mA

+3.3V_TBT_R — RT88 — +3.3VA_TBT_R

EVT2_41 — CT304 10U_0402_10V6M @, CT305 18P_0201_25V8J, CT81 1U_0201_6.3V6K

Place near Pin J7
3.3v @ 50mA

+TBT_R_SVR_IND — LT5 0.68UH_MLV-YT10NR68N-M1L_2.7A_30%

EVT2_41 — +0.9V_TBT_R_SVR

CT73 1U_0201_6.3V6K @, CT74 1U_0201_6.3V6K @, CT75 1U_0201_6.3V6K, CT76 1U_0201_6.3V6K, CT77 1U_0201_6.3V6K, CT78 1U_0201_6.3V6K @, CT79 47U_0603_6.3V6M, CT80 18P_0201_25V8J

DVT1_06

Place near Pin F6,G6,E3,G3,E9,G9
GND share with Pin M2, M3
0.9v @ 850mA

DVT1_53 BB ref sch Rev 1.4 change to CAP Place near Pin F6,E3,E9 G3,G6,G9 CAP change to NC

+3VALW — CT211 1U_0201_6.3V6K

UT2 — AOZ1336DI_DFN8_2X2

(44) PD_TCP2_LS_EN	RT94 1 @ 2 0_0201_5%		
(11,16,47,58) SIO_SLP_SUS#	RT95 1 @ 2 0_0201_5%	3.3V_TBT_R_EN	
		VIN_1	VOUT_1 — +3.3V_TBT_R_B — LT15 EMI@ BLM18KG331SN1D_2P — 3.3v @ 370mA +3.3V_TBT_R
		VIN_2	VOUT_2
		ON	CT — CT210 470P_0402_50V7K
		VBIAS	
			GND_1, GND_2

+3.3V_TBT_R — CT212 0.1U_0201_10V6K

EVT2_34

3.3V_TBT_R_EN	RT93 1 2 100K_0201_5%	
	RT158 1 @ 2 10K_0201_5%	+3VALW

BB ref sch p.6 note
DG_P1_PWR_GATE_EN:

For PD based systems, DG_P1_PWR_GATE_EN should be output from PD.

For TCPC based systems, DG_P1_PWR_GATE_EN should be output from SOC/EC.

URT2C — BURNSIDE-BRIDGE_BGA105 @

B1	VSS_ANA_1	VSS_ANA_12	F12
B12	VSS_ANA_2	VSS_ANA_13	G7
D1	VSS_ANA_3	VSS_ANA_14	H1
D2	VSS_ANA_4	VSS_ANA_15	H2
D11	VSS_ANA_5	VSS_ANA_16	H11
D12	VSS_ANA_6	VSS_ANA_17	H12
F1	VSS_ANA_7	VSS_ANA_18	J9
F2	VSS_ANA_8	VSS_ANA_19	K1
F7	VSS_ANA_9	VSS_ANA_20	K2
F9	VSS_ANA_10	VSS_ANA_21	K11
F11	VSS_ANA_11	VSS_ANA_22	K12
	GND	VSS_1	G5
		VSS_2	F5
		VSS_3	F3

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

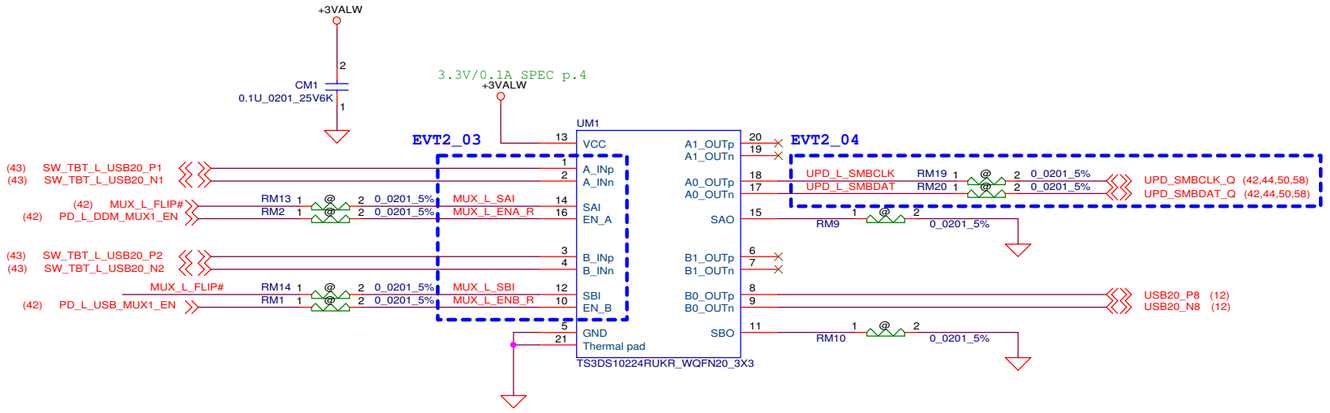
Compal Electronics, Inc.

Title: P049 - TYPE-C TBT_BB R_PWR,GND

Size | Document Number: LA-G172P | Rev: 1.0 (A00)

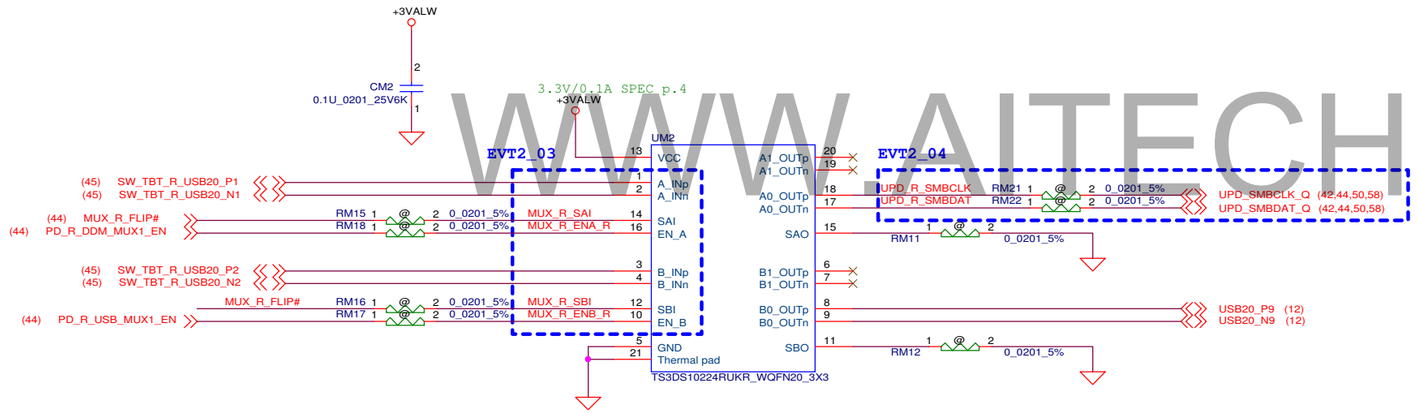
Date: Friday, May 24, 2019 | Sheet 49 of 101

USB2/I2C MUXES_L



EVT1_17

USB2/I2C MUXES_R



ENA, ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	Hi-Z	Hi-Z	Hi-Z	Hi-Z
01	Hi-Z	Hi-Z	–	–
10	–	–	Hi-Z	Hi-Z
11	–	–	–	–

SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	–	INA	–
0001	INB	–	–	INA
0010	INB	–	INB	–
0011	INB	–	–	INB
0100	–	INB	INA	–
0101	–	INB	–	INA
0110	–	INB	INB	
0111	–	INB	–	INB
1000	INA	–	INA	–
1001	INA	–	–	INA
1010	INA	–	INB	–
1011	INA	–	–	INB
1100	–	INA	INA	–
1101	–	INA	–	INA
1110	–	INA	INB	–
1111	–	INA	–	INB

Channel	INA	INB
Signal Name	TOP	BOT

					I2C	USB		
ENA	ENB	SAI	SBI	SAO	OUTA0	OUTB0	Mux Functional Mode	PD Controller W/DDM
0	1	–	0	–	Hi-Z	TOP	–	USB only on TOP
0	1	–	1	–	Hi-Z	BOT	–	USB only on BOT
1	1	0	0	0	BOT	TOP	Crosspoint Switch	USB on TOP W/DDM
1	1	1	1	0	TOP	BOT	Crosspoint Switch	USB on BOT W/DDM

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P050 - TYPE-C USB/I2C MUX
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
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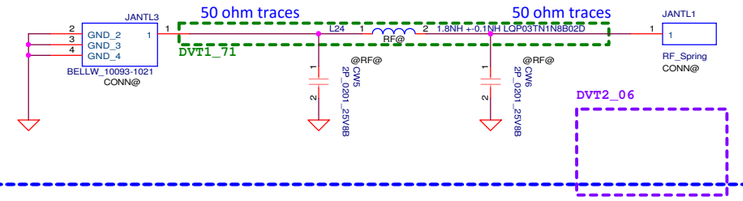
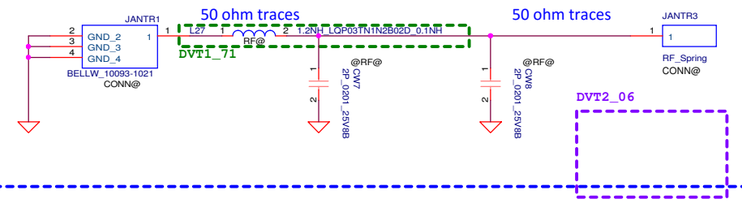
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

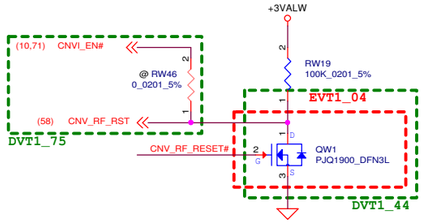
Compal Electronics, Inc.		
Title: ***P051 - Reserve***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 51 of 101	

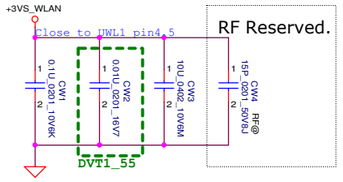
Reserved for RF Antenna L debug

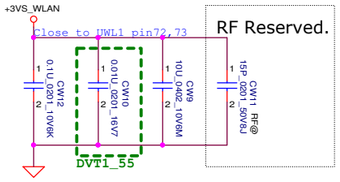


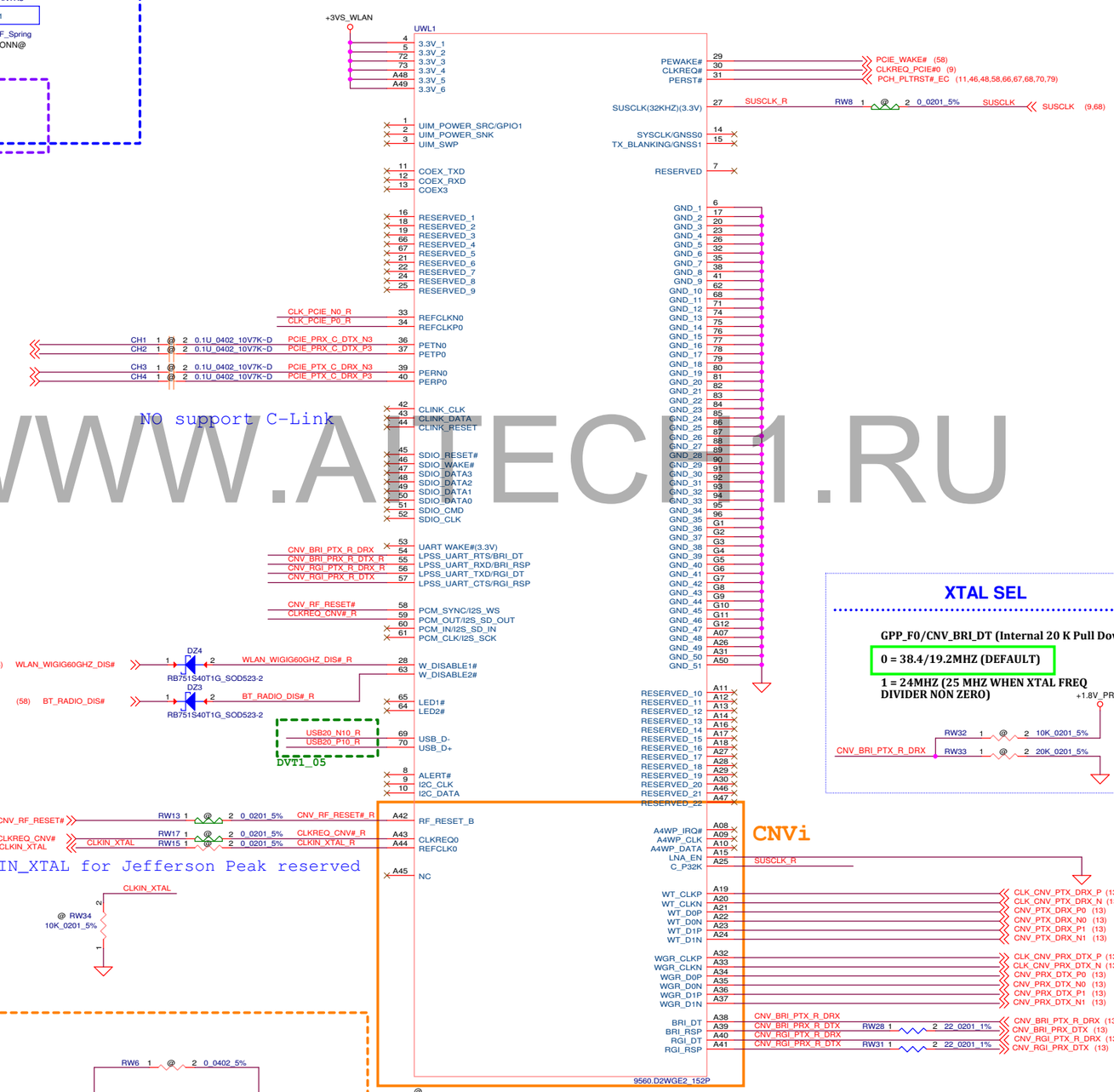
Reserved for RF Antenna R debug









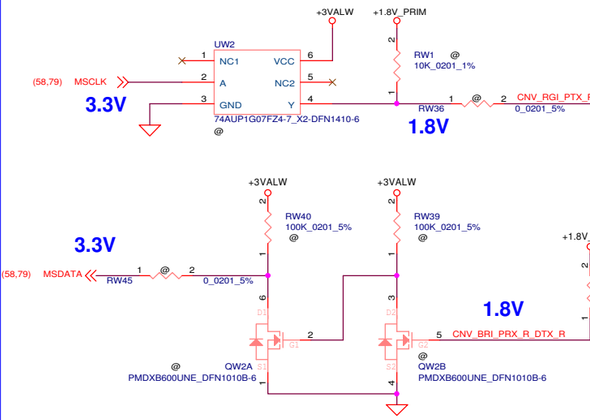


NO support C-Link

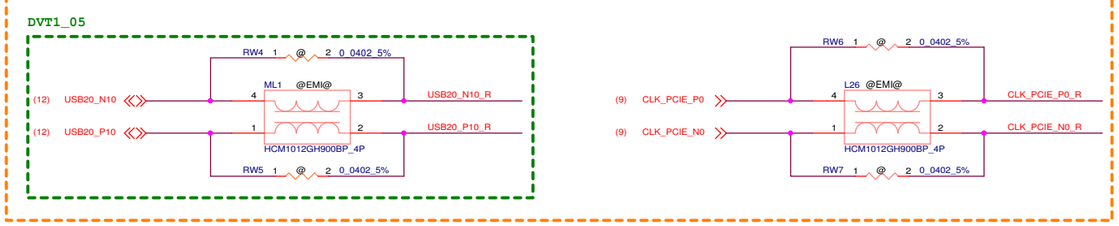
CLKIN_XTAL for Jefferson Peak reserved

CNVi&KILLER BOM option co-lay

EC Side
MSCLK:TX
MSDATA:RX
If pop KIEER@ components ,
RE205 need de-pop



DVT1.2_17



XTAL SEL

GPP_F0/CNV_BRI_DT (Internal 20 K Pull Down)

0 = 38.4/19.2MHZ (DEFAULT)

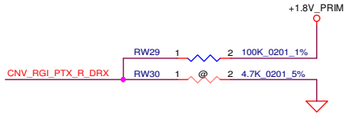
1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

M.2 CNVI MODES

GPP_F2/CNV_RGI_DT

0 = INTEGRATED CNVI ENABLE

1 = INTEGRATED CNVI DISABLE



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P052 - WLAN/BT (w/ CNVi)
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
Sheet	52 of 101

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title	***P053 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 53 of 101	

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title	***P054 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 54 of 101	

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title: ***P055 - Reserve***		
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Beep sound

RC filter for PWM square to sine-wave

(58) BEEP — RA8 1K_0201_5% — RA27 0_0201_5% — RA28 0_0201_5% — CA14 0.1U_0201_10V6K — MONO_IN

CA46 0.22U_0201_6.3V6M — CA47 0.22U_0201_6.3V6M — CA48 0.22U_0201_6.3V6M

(10) SPKR — RA9 1K_0201_5% — RA30 1K_0201_5% — CA13 100P_0201_25V7K

Close to UA1 Pin32

Close Audio jack

TOP: RA22 0_0402_5%; CA78 @EMI@ 0.1U_0402_10V7K

BOT: RA23 0_0402_5%; CA79 @EMI@ 0.1U_0402_10V7K

Close Codec

RA25 0_0402_5%; CA80 @EMI@ 0.1U_0402_10V7K; CA81 @EMI@ 0.1U_0402_10V7K

Place on Codec to Audio Jack Path

CA83 @EMI@ 0.1U_0402_10V7K; CA82 @EMI@ 0.1U_0402_10V7K

GND — Moat — AGND

Don't short this pad to USB digital ground, and should be far away from any power traces.

Codec AVDD (Placement near Audio Codec)

+AVDD1 — LA1 HCB2012KF-600T30 — +5VS_AUDIO

ANALOG | DIGITAL

CA19 10U_0402_10V6M — AGND

DA11 AZ5125-01H.R7G_SOD523-2 — EMI@

Moat

In order to prevent the built-in LDO damaged from over-voltage on +5VD or Standby power line, we suggested using this Voltage suppressing device.

10 mA

+3VS_AUDIO — RA29 0_0402_5%

+1.8VS_AUDIO — RA36 0_0402_5% — +DVDD

CA39 10U_0402_6.3V6M — CA33 0.1U_0201_10V6K

CA39, CA33 close with UA1 Pin3

5 mA

+3VS_AUDIO — RA18 0_0402_5%

+1.8VS_AUDIO — RA41 0_0402_5% — +DVDDIO

CA38 10U_0402_6.3V6M — CA36 0.1U_0201_10V6K

CA38,CA36close with UA1 Pin18

200 mA

+AVDD1 — Place next to CODEC — CA22 10U_0402_10V6M — CA23 0.1U_0201_10V6K — AGND

3 A

Add this Filter to avoid other components/chips be influenced

+5VS_AUDIO — LA2 HCB1608KF-121T30_0603 — +PVDD

CA62 10U_0402_10V6M — CA63 0.1U_0201_10V6K

CA25 10U_0402_10V6M — CA26 0.1U_0201_10V6K

CA25,CA26 close to UA1 pin41

1.5 A

+PVDD

CA31 10U_0402_10V6M — CA30 0.1U_0201_10V6K

CA31,CA30 close to UA1 pin46

R0 is 100K ohm.

3.3V — 0.5R R0 — R R1 (HP JD resister) — GND

JACK DETECTION NETWORK

+DVDD — RA13 100K_0201_1% — JACK_PLUG# — RA14 200K_0201_1% — CA40 @ 0.1U_0201_10V6K — (57) HP_PLUG#

Internal pull high to +DVDD

0_0201_5% — RA66 — DA10 RB751S40T1G_SOD523-2 — (58) NB_MUTE# — CODEC_MUTE# — RA21 @ 1K_0201_5%

ALC3281-CG

QFN48(6*6)

Thermal pad=DGND

Powered by AVDD1 / Powered by CPVDD/AVDD2 / Powered by PVDD / Powered by DVDD-IO / Powered by DVDD

AVSS1 VREF LDO1_CAP AVDD1 PVDD1 SPKL+ SPKL- SPKR+ SPKR- PVDD2 JD2 JD1 GND

CBN CBP AVSS2 LDO2_CAP CPVDD/AVDD2 LDO3_CAP DVDD_IO SDATA_OUT SDATA_IN SYNC BCLK SPDIF/EAPD

LINE2-L LINE2-R PCBEEP JDREF MIC_CAP SLEEVE RING2 MIC2-VREFO-R MIC2-VREFO-L HPOUT-L HPOUT-R CPVEE

GPIO2/DMIC-DATA-12 GPIO1/DMIC-CLK SCL SDA DVDD GPIO0/DMIC-DATA-34/I2S OE

(57) SPK_OUT-L+ (57) SPK_OUT-L- (57) SPK_OUT-R- (57) SPK_OUT-R+

JACK_PLUG#

AGND — CA17 2.2U_0201_10V6K — EVT1_21 — RA10 100K_0201_5% — CA20 4.7U_0402_10V6M

+AVDD1 — RA64 10K_0201_5% — CA15 10U_0402_10V6M

LINE2-L (57) — LINE2-R (57) — SLEEVE (57) — RING2 (57) — MIC2-VREFO-R (57) — MIC2-VREFO-L (57) — HPOUT-L (57) — HPOUT-R (57)

CPVEE — CA18 2.2U_0603_10V7K — AGND

0603 type

Place near UA1 pin26/27

HPOUT-R — CA9 330P_0201_50V7K — AGND

HPOUT-L — CA11 330P_0201_50V7K — AGND

0603 type

CBN — CBP — CA21 2.2U_0603_10V7K — AGND

LDO2_CAP — CA51 10U_0402_10V6M — AGND

1.8V power rail should be supplied by linear regulator, not switching regulator. If switching regulator is unavoidable, Please make sure that switching frequency operates at out- band(over 20KHz).

50 mA

+1.8VS_AUDIO

Near Codec — LDO3_CAP — CA32 10U_0402_10V6M — +DVDDIO

CA424 0.1U_0201_10V6K — CA429 10U_0402_10V6M — AGND

HDA_SDIN0_L — RA17 33_0201_5% — HDA_SDIN0 (10)

HDA_SDOUT_L (10) — HDA_SYNC_L (10) — HDA_BIT_CLK_L (10)

CA37 @ 22P_0201_25V8

+DVDD — RA63 0_0201_5%

100K Necessary — RA57 100K_0201_5% — CODEC_MUTE#

DVT1_19 — CA55 @ U_0201_6.3V6M

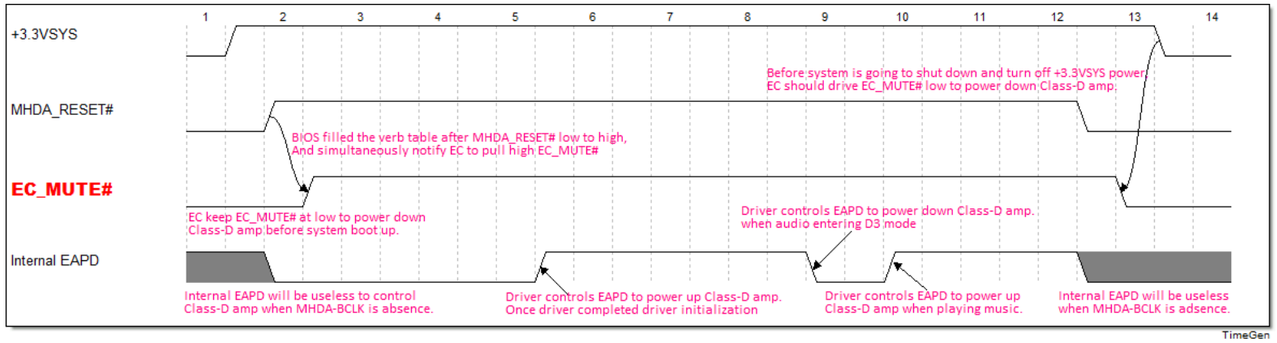
(39) DMIC_DATA12 — RA58 0_0201_5% — DMIC_DATA12_R

(39) DMIC_CLK12 — RA62 22_0201_5% — DMIC_CLK12_R

CA57 10P_0201_50V8J EMI@ — CA64 @EMI@ 33P_0201_50V8J

Near Codec pin5

The PDB control timing by EC_MUTE#



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P056 - Audio ALC3281			
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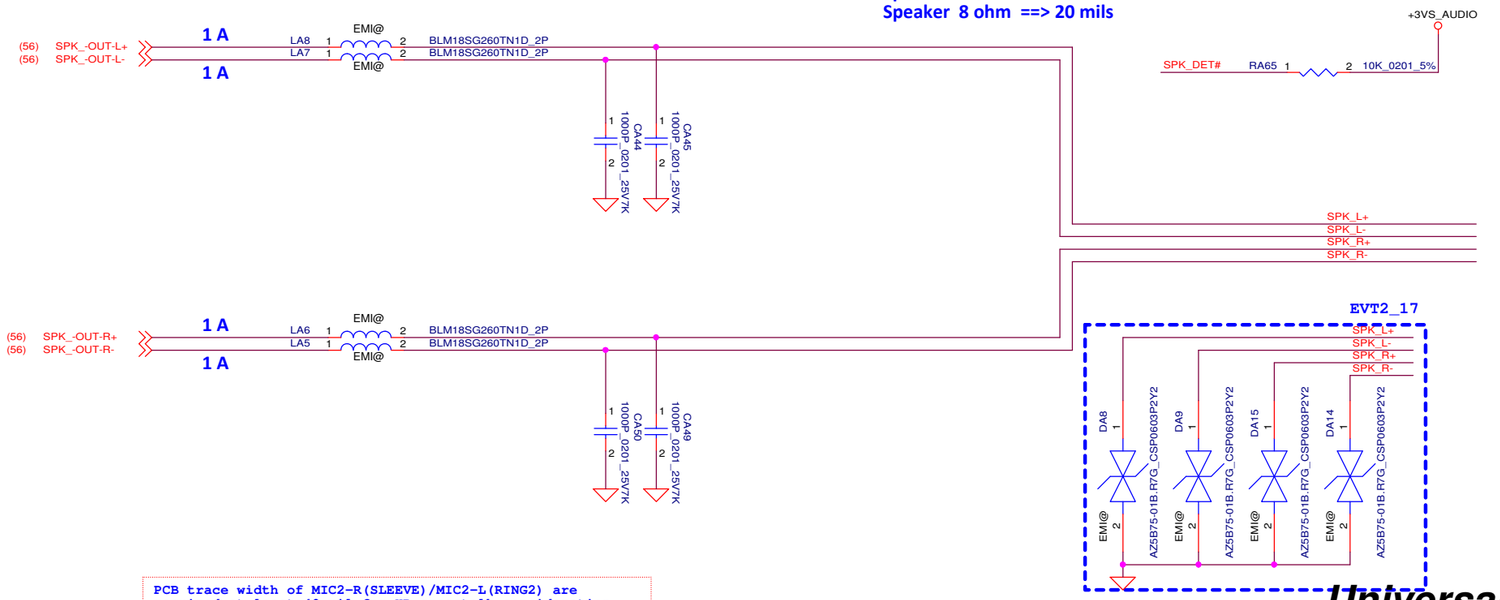
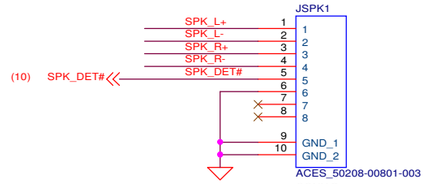
Int. Speaker Conn.

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils



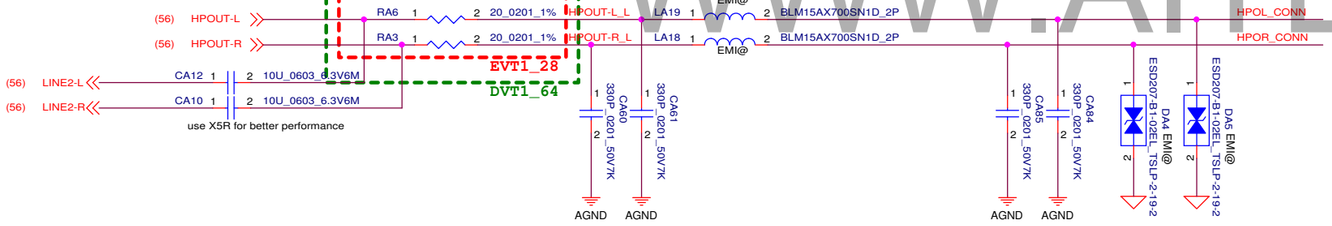


PCB trace width of MIC2-R(SLEEVE)/MIC2-L(RING2) are required at least 40 mil for HP crosstalk consideration and, its length should be as short as possible.
LA19/L15 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk.

Universal Audio Jack CONN

Universal Audio Jack

change RA6/RA3 to 5.6 ohm to meet Dell Grade A heapdhone output power > 25 mW setting



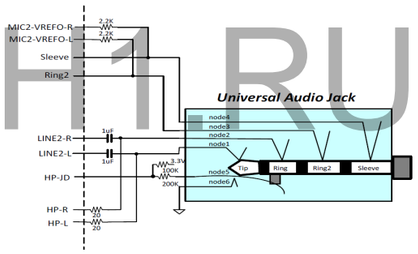
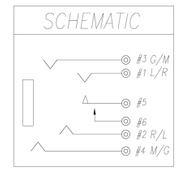
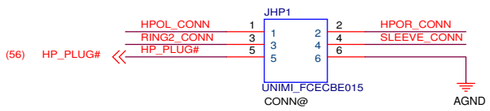
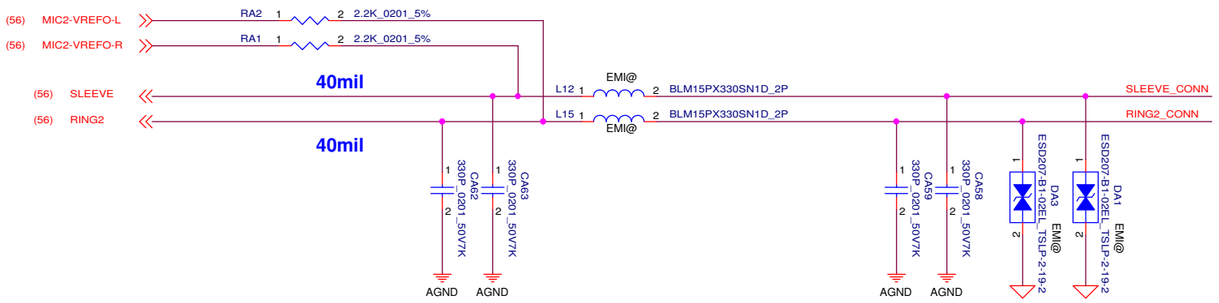


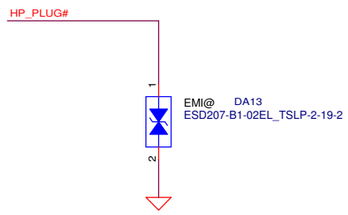
Figure 2. Analog Connector and Device





Contact with PC BEAN





Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P057 - Audio Jack/Speaker			
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S5 LID OPEN POWER ON

POWER SW

NB LID/TAB LID

Touch Pad PS2

Connect to PCH

Reserved for debug

Charger and Battery

PD

VCCIN VR

System crash protection

Setting for Thermal Design

Thermal diode mapping

MEC5105 pins	thermal diode	Location
DP1/DN1	QE4	CPU(OTP)
DN1a/DP1a	QE14	DDR
DP2/DN2	QE17	SSD
DN2a/DP2a	QE8	WLAN
DP3/DN3	QE10	Charger
DN3a/DP3a	QE3	Ambient
DP4/DN4	Reserved	Reserved
DN4a/DP4a	---	---

FUNCTION TABLE

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

RE194	CE75	REV
240K	4700p	M00
130K	4700p	X00
62K	4700p	X01
33K	4700p	X02
8.2K	4700p	X03
4.3K	4700p	X04
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

RE525	CE432	CPU TYPE
240K	4700p	Non V-PRO I3
130K	4700p	Non V-PRO I5
62K	4700p	Non V-PRO I7
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

Stuff RE185 and no stuff RE186 keep E5 design
Stuff RE186 and no stuff RE185 to save two GPIOs on EC(PCH_PCIE_WAKE# should be output with OD)

RE147 close to UE1 at least 250mils

Rest=1.58K , Tp=96 degree

ESPI only support 1.8V

Close to pin H1

Close to pin N5

close to pin G8/M9

Amber
White

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Compal Electronics, Inc.

Title: P058 - EC MEC5105

Document Number: LA-G172P

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Compal Electronics, Inc.		
Title	***P059 - Reserve***	
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Compal Electronics, Inc.		
Title	***P060 - Reserve***	
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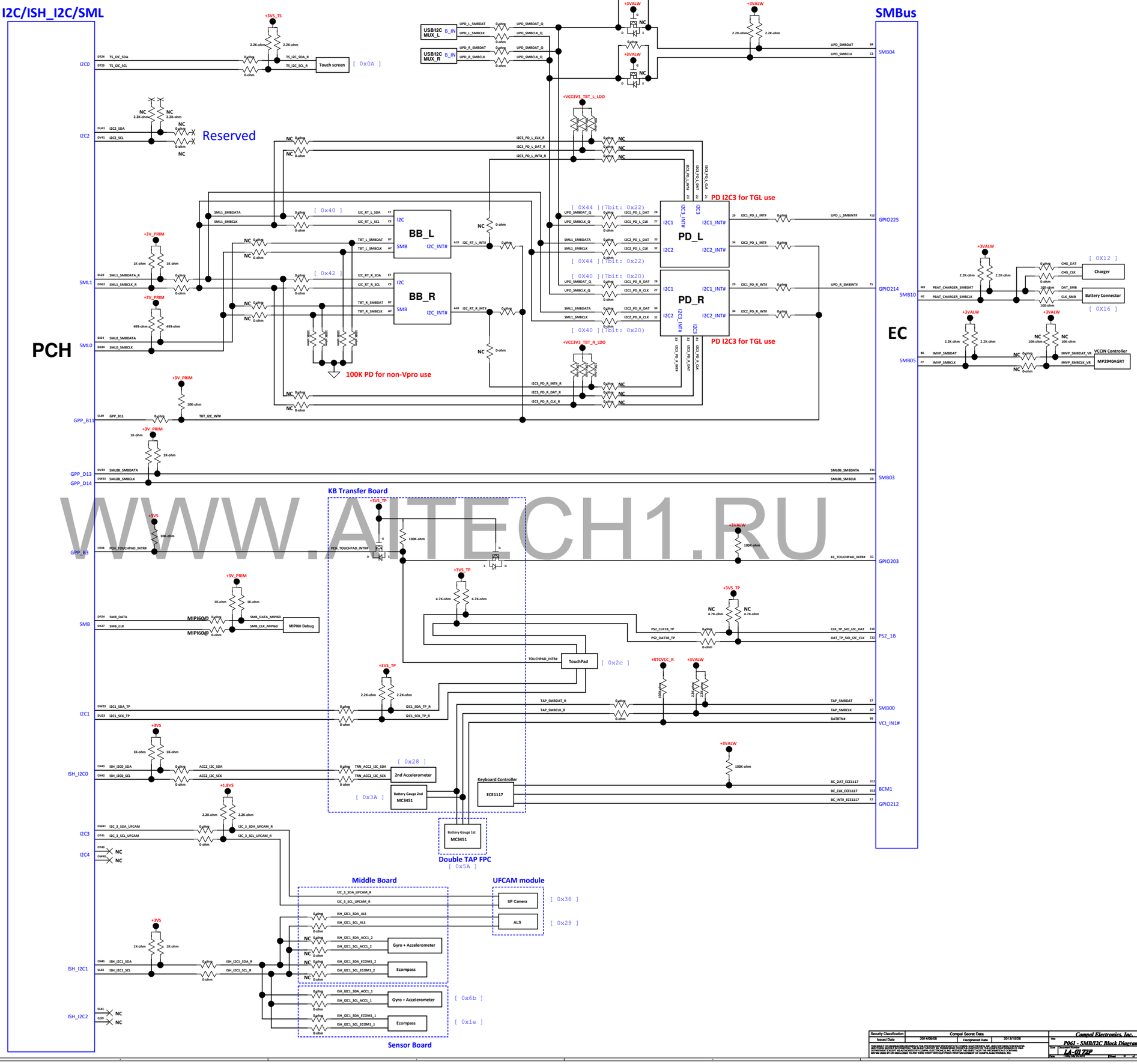
I2C/ISH_I2C/SML
SMBus
PCH
EC
I2C0
I2C2
SML1
SML0
GPP_B11
GPP_D13
GPP_D14
GPP_B3
SMB
I2C1
ISH_I2C0
I2C3
I2C4
ISH_I2C1
ISH_I2C2
SMB04
GPIO225
GPIO214
SMB10
SMB05
SMB03
GPIO203
PS2_1B
SMB00
VCI_IN1#
BCM1
GPIO212
Touch screen
[0x0A]
Reserved
PD I2C3 for TGL use
PD_L
PD_R
BB_L
BB_R
100K PD for non-Vpro use
Charger
Battery Connector
[0x12]
[0x16]
VCCIN Controller
MP2940AGRT
KB Transfer Board
MIPI60 Debug
TouchPad
[0x2c]
2nd Accelerometer
[0x28]
Battery Gauge 2nd
MC3451
[0x3A]
Keyboard Controller
ECE1117
Battery Gauge 1st
MC3451
Double TAP FPC
[0x5A]
Middle Board
UFCAM module
UF Camera
[0x36]
ALS
[0x29]
Gyro + Accelerometer
Ecompass
[0x6b]
[0x1e]
Sensor Board
WWW.AITECH1.RU
Compal Electronics, Inc.
P061 - SMB/I2C Block Diagram
LA-G172P

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Compal Electronics, Inc.		
Title	***P062 - Reserve***	
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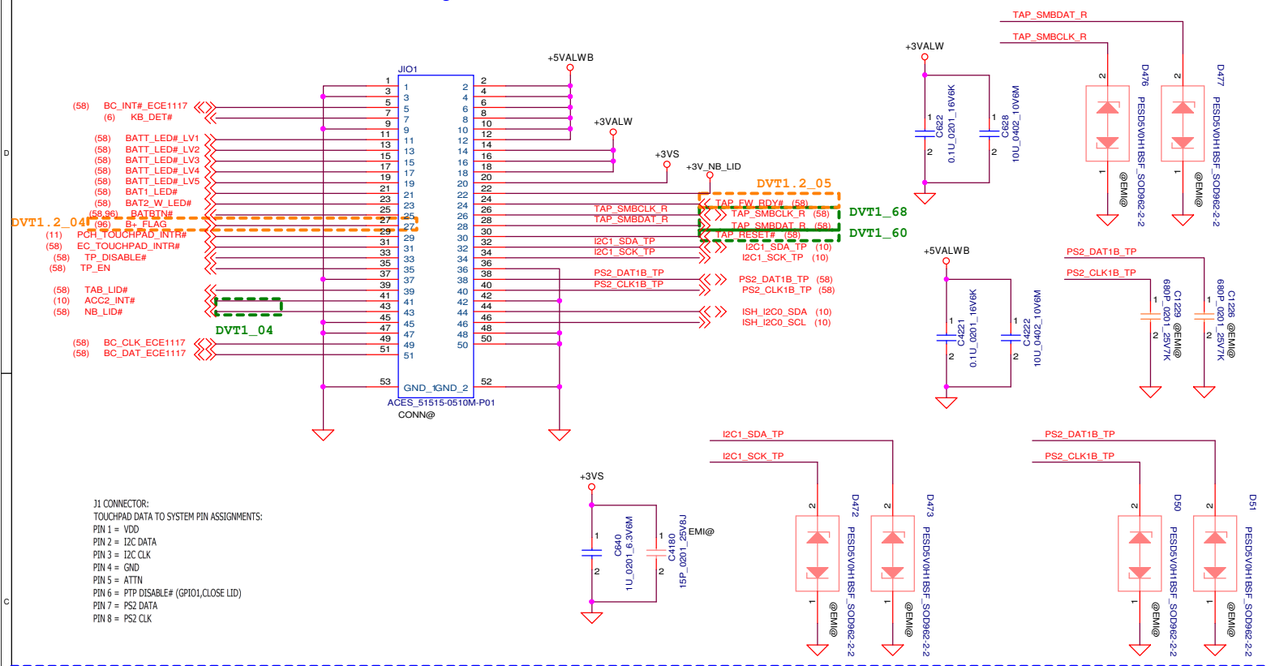
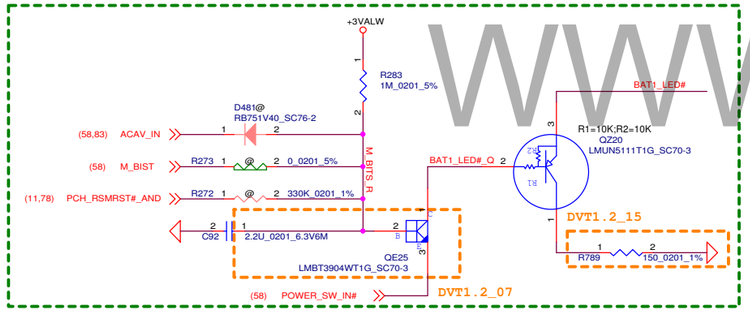
KB Controller & TP transfer Conn

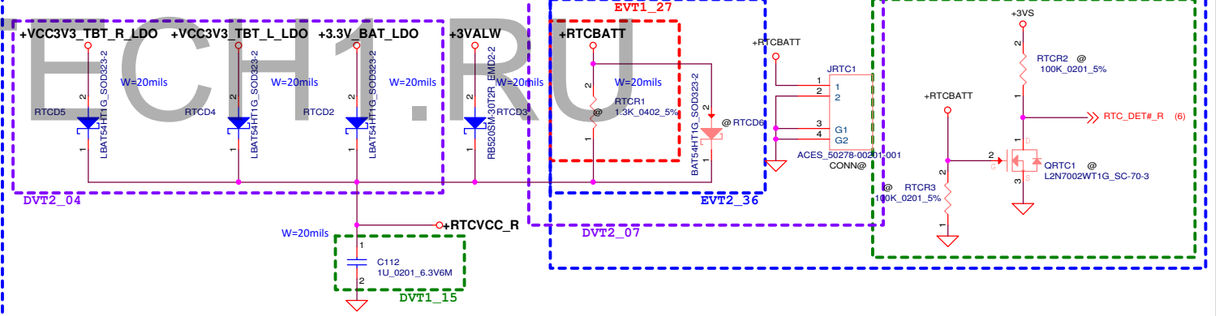


J1 CONNECTOR:
TOUCHPAD DATA TO SYSTEM PIN ASSIGNMENTS:
PIN 1 = VDD
PIN 2 = I2C DATA
PIN 3 = I2C CLK
PIN 4 = GND
PIN 5 = ATTN
PIN 6 = PTP DISABLE# (GPIO1,CLOSE LID)
PIN 7 = PS2 DATA
PIN 8 = PS2 CLK

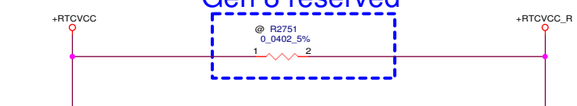
M-BIST



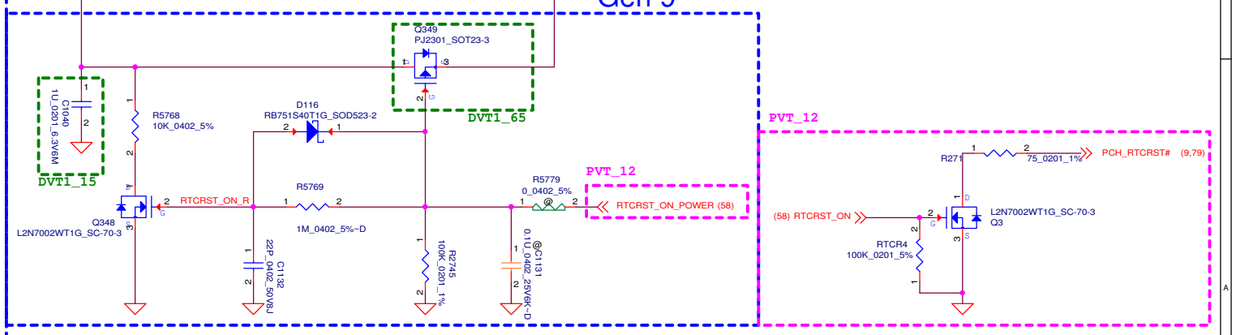
RTC



Gen 8 reserved



Gen 9



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.	
Title	P063 - KB/TP/RTC
Size	Document Number: LA-G172P
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Compal Electronics, Inc.

Title: **P064 - Reserve**

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Compal Electronics, Inc.		
Title	***P065 - Reserve***	
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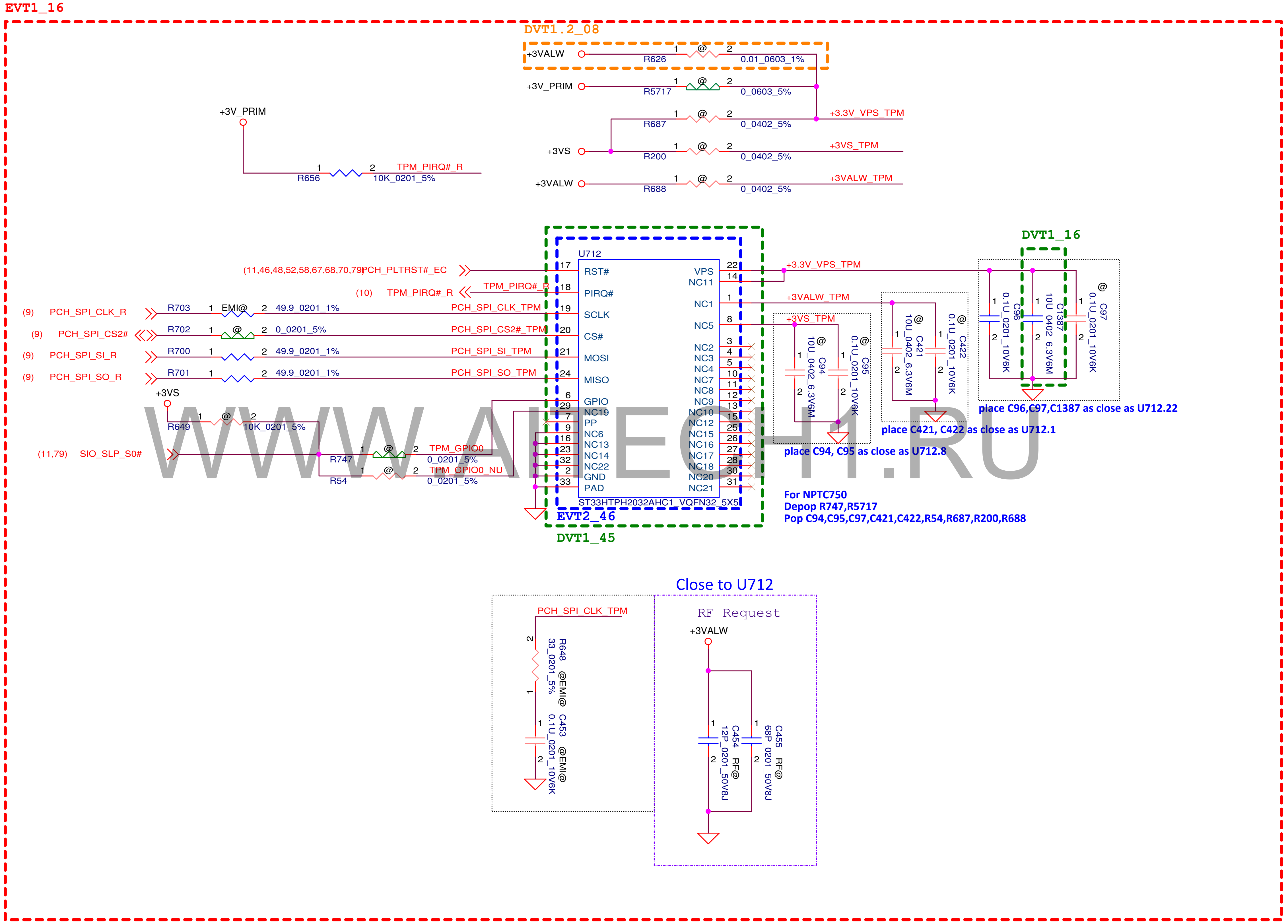
For ST TPM



EVT1_16
DVT1.2_08
+3VALW
R626
0.01_0603_1%
+3V_PRIM
R5717
0_0603_5%
R687
0_0402_5%
+3.3V_VPS_TPM
+3VS
R200
+3VS_TPM
R688
+3VALW_TPM
R656
10K_0201_5%
TPM_PIRQ#_R
U712
(11,46,48,52,58,67,68,70,79) PCH_PLTRST#_EC
(10) TPM_PIRQ#_R
(9) PCH_SPI_CLK_R
(9) PCH_SPI_CS2#
(9) PCH_SPI_SI_R
(9) PCH_SPI_SO_R
R703
R702
R700
R701
49.9_0201_1%
0_0201_5%
PCH_SPI_CLK_TPM
PCH_SPI_CS2#_TPM
PCH_SPI_SI_TPM
PCH_SPI_SO_TPM
RST#
PIRQ#
SCLK
CS#
MOSI
MISO
GPIO
PP
GND
PAD
VPS
NC11
NC1
NC5
ST33HTPH2032AHC1_VQFN32_5X5
R649
10K_0201_5%
(11,79) SIO_SLP_S0#
R747
R54
TPM_GPIO0
TPM_GPIO0_NU
EVT2_46
DVT1_45
DVT1_16
C94
C95
C421
C422
C96
C1387
C97
place C96,C97,C1387 as close as U712.22
place C421, C422 as close as U712.1
place C94, C95 as close as U712.8
For NPTC750
Depop R747,R5717
Pop C94,C95,C97,C421,C422,R54,R687,R200,R688
Close to U712
R648 33_0201_5% @EMI@
C453 0.1U_0201_10V6K @EMI@
RF Request
C454 12P_0201_50V8J RF@
C455 68P_0201_50V8J RF@

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title: P066 - TPM

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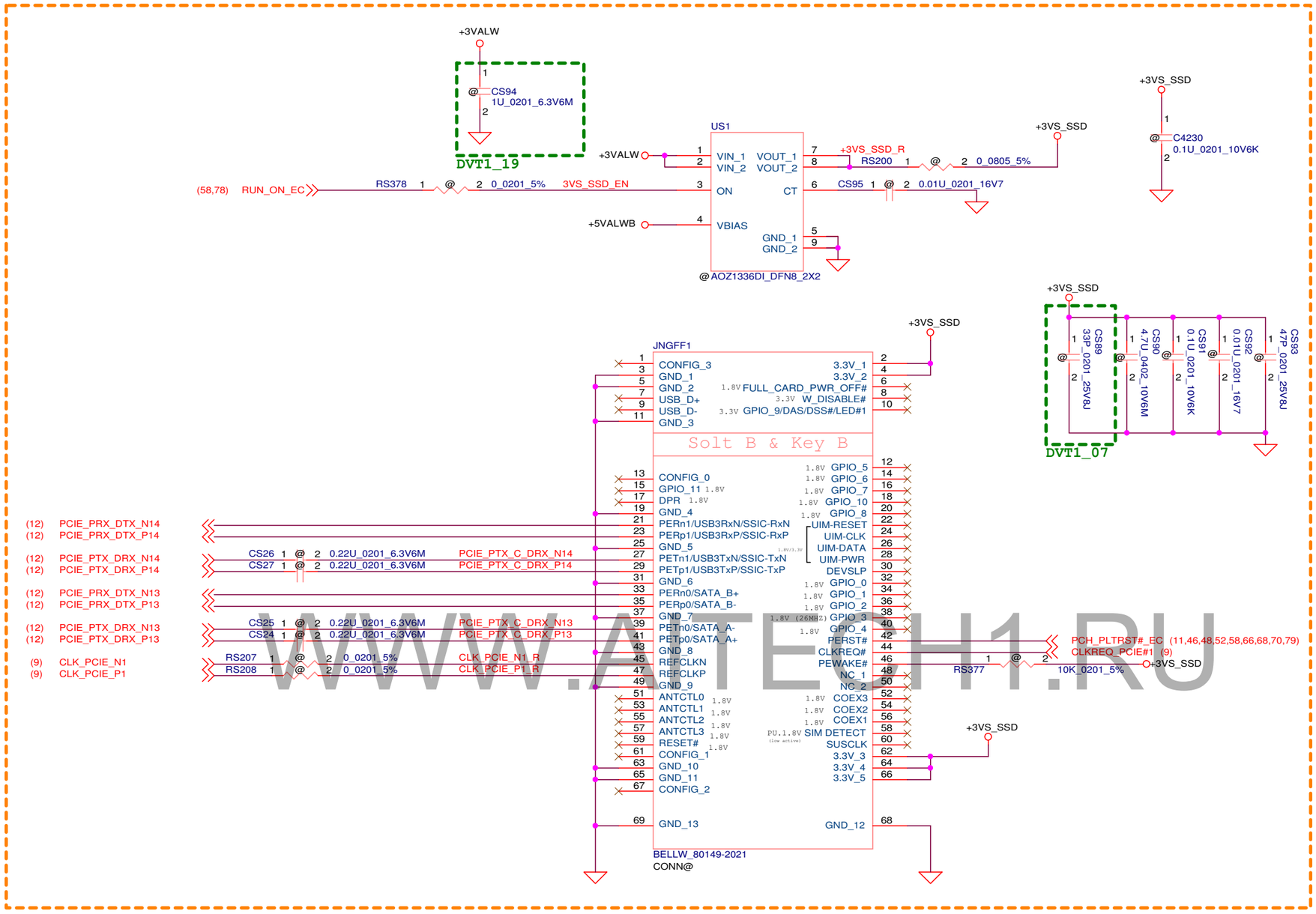

DVT1.2_16

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P067 - M.2 SSD CONN Reserve			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
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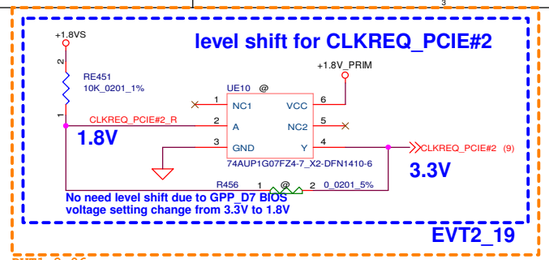
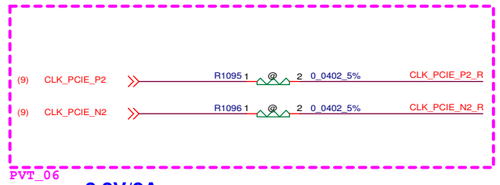
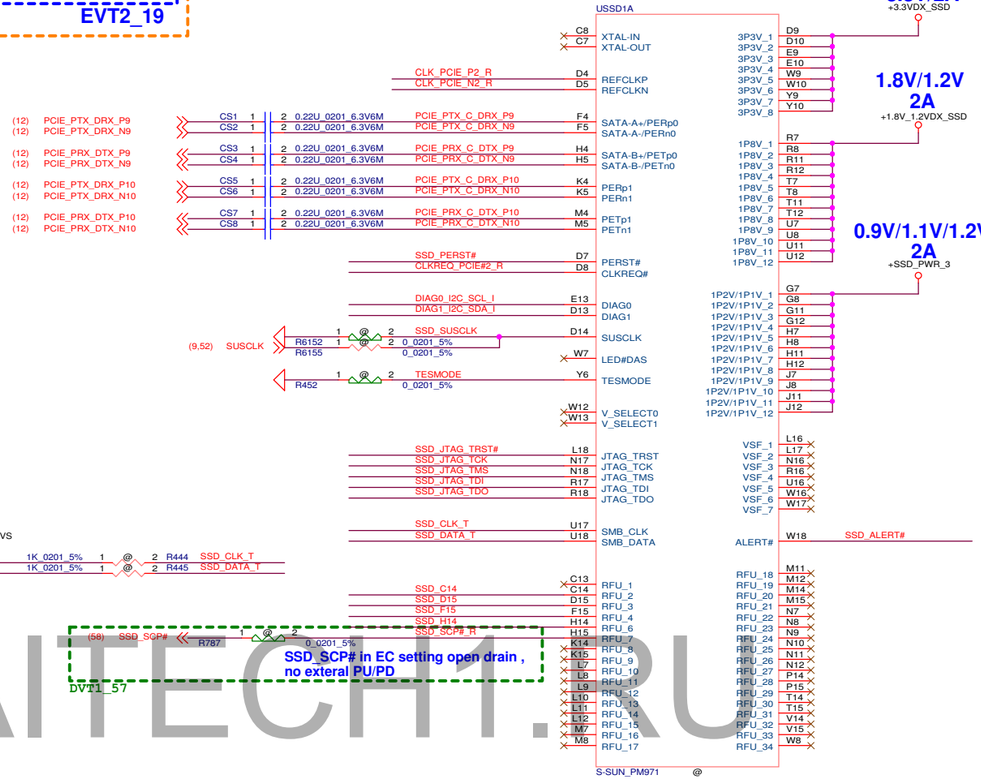
Power Rail Configuration Pins for 16x20 BGA SSD

PWR_2		PWR_3			
C14	Voltage	D15	F15	H14	Voltage
GND	1.8V	GND	NC	NC	0.9V
NC	1.2V	NC	GND	NC	1.1V
		NC	NC	GND	1.2V



SSD_PERST#	CLKREQ_PCIE#2_R	SSD_SUSCLK
1.8V	1.8V	GND



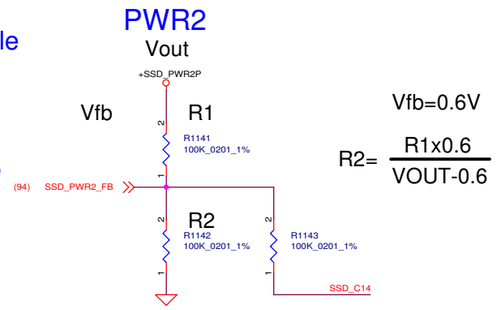


PWR2 BOM option power select table

+SSD_PWR2P	R1142	R1143
1.8V	49.9K	Non-POP
1.2V	100K	Non-POP

PWR2 SSD C14 power select table (All component POP)

+SSD_PWR2P	SSD_C14
1.8V	GND
1.2V	NC

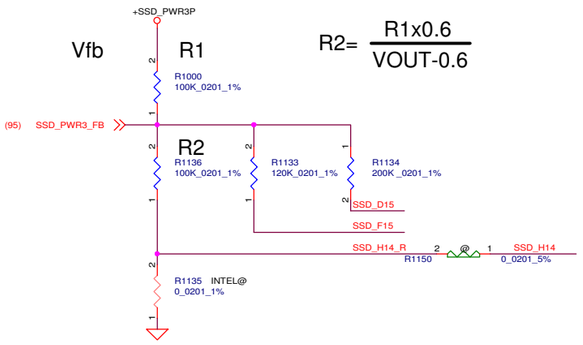


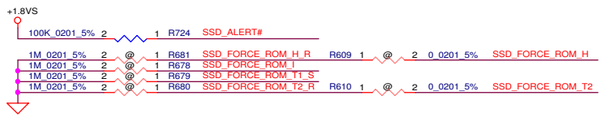
PWR3 BOM option power select table

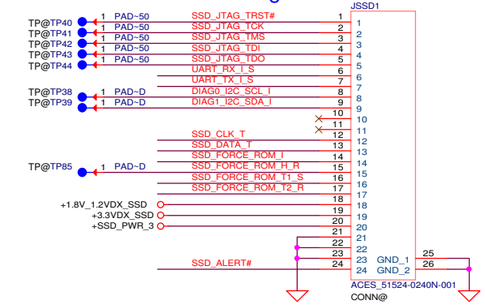
+SSD_PWR3P	R1136	R1133	R1134	R1135	R1150
0.9V	200K	Non-POP	Non-POP	POP	Non-POP
1.1V	120K	Non-POP	Non-POP	POP	Non-POP
1.2V	100K	Non-POP	Non-POP	POP	Non-POP

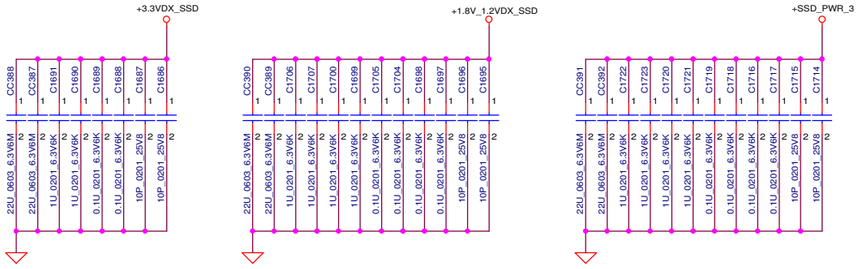
PWR3 SSD CFG power select table (All component POP , except R1135)

+SSD_PWR3P	SSD_D15	SSD_F15	SSD_H14	R1135	R1150
0.9V	GND	NC	NC	Non-POP	POP
1.1V	NC	GND	NC	Non-POP	POP
1.2V	NC	NC	GND	Non-POP	POP

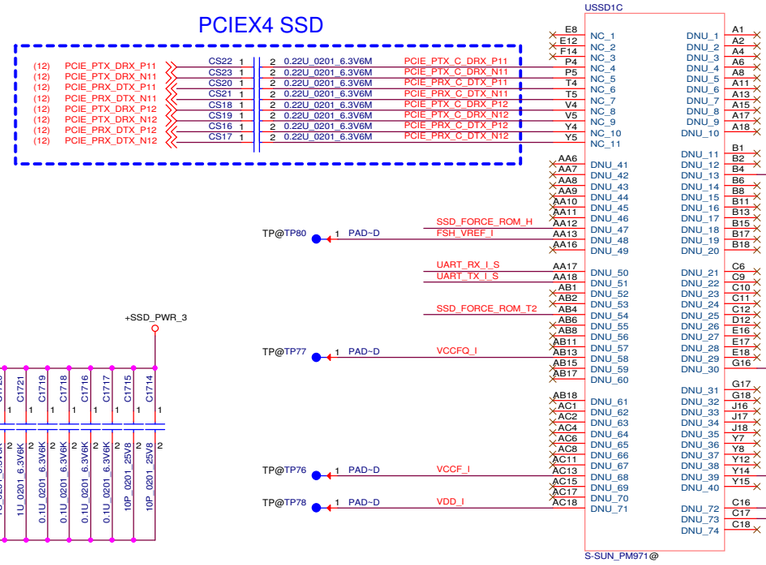








PCIEX4 SSD



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

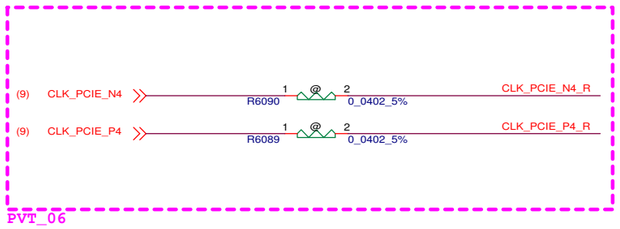
Compal Electronics, Inc.	
Title	P068 - 1620 BGA SSD
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date: Friday, May 24, 2019	Sheet 68 of 101

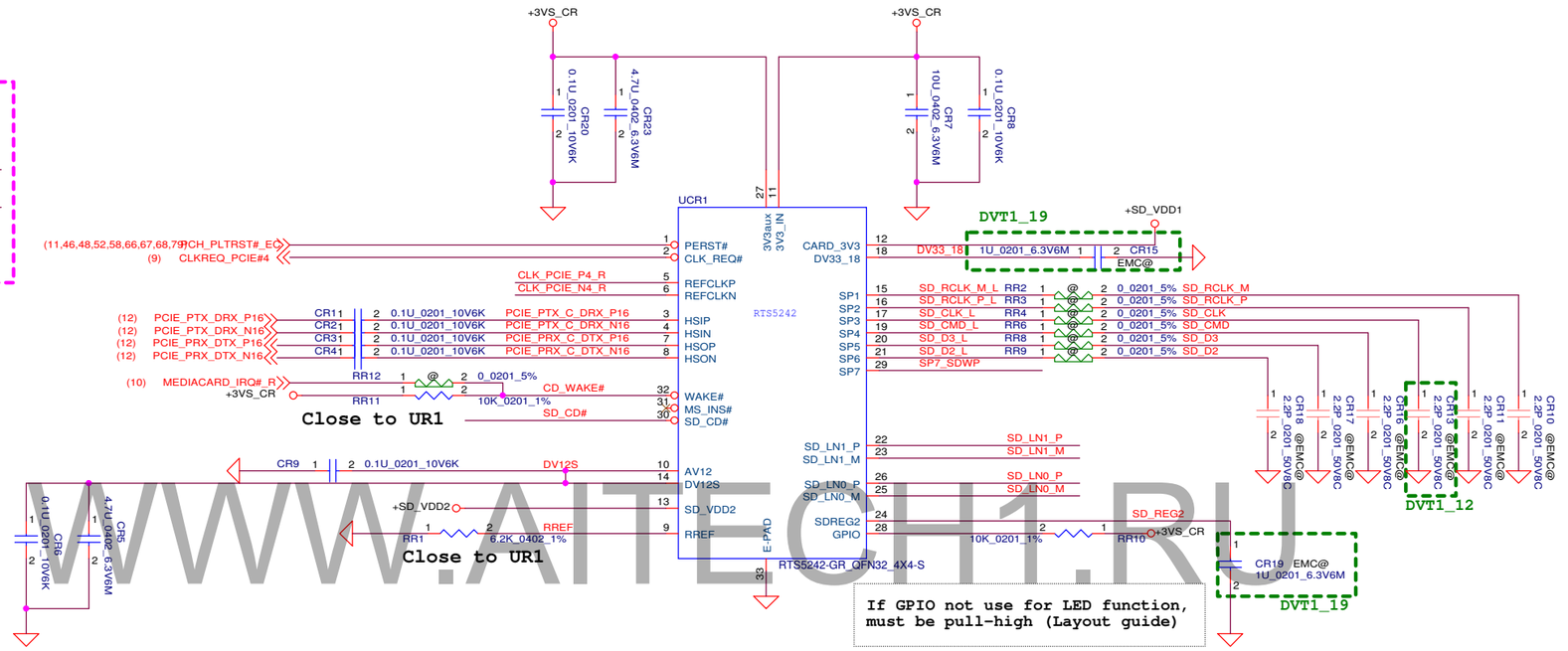
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

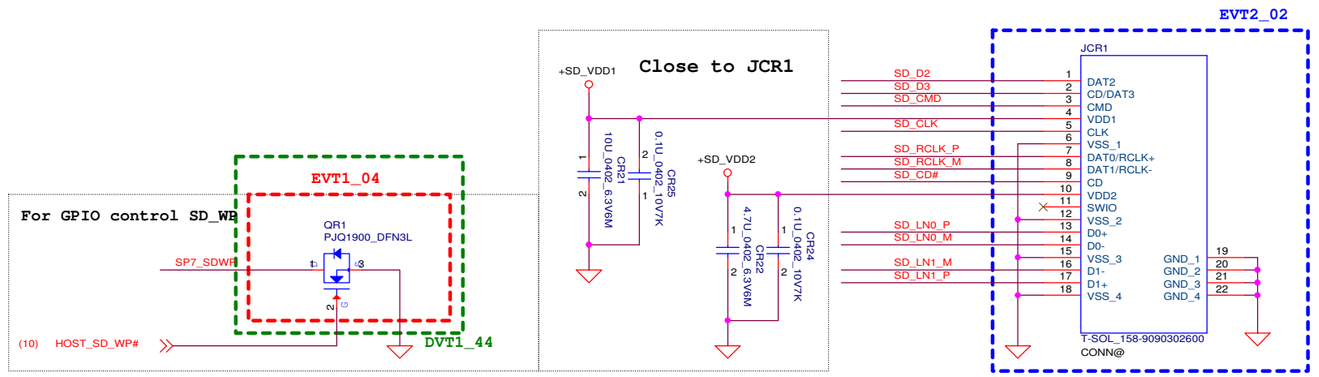
Compal Electronics, Inc.		
Title	***P065 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 69 of 101	

Card Reader

1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
   - Bulk capacitor for Card_3V3 place closed to flash card socket.
   - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



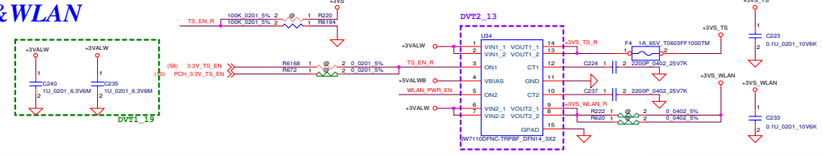




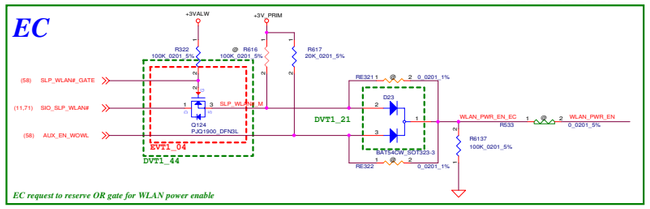
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P070 - Card reader uSD RTS5242		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
Date:	Friday, May 24, 2019	Sheet	70 of 101

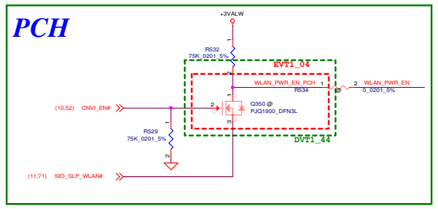
TS&WLAN



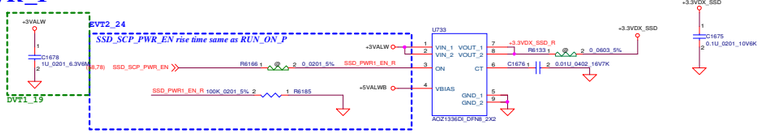
EC



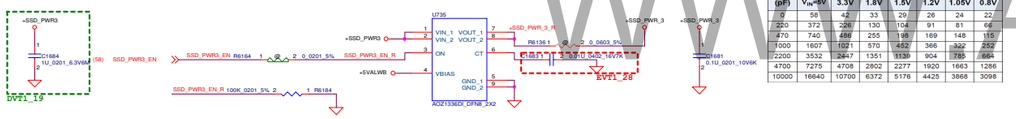
PCH



SSD_PWR_1

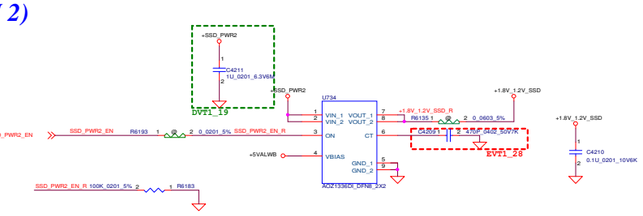


SSD_PWR_3

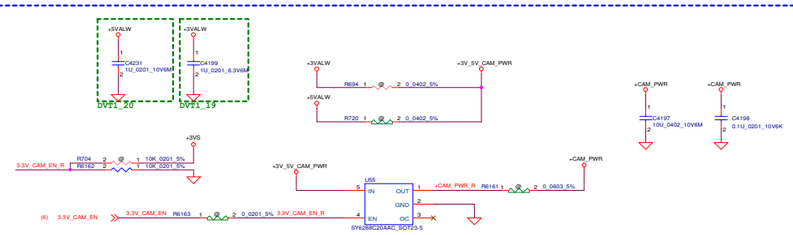


C_L (pF)	Rise Time (μs) 10%~90% C_L=0.1μF, C_{SS}=1μF, R_L=10Ω (Typical values) at 25°C, 3V X7R 10% Ceramic Cap)						
	V_{IN}=5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	58	42	33	29	26	24	22
220	372	226	130	104	91	81	66
470	740	486	255	198	169	148	115
1000	1607	1021	570	452	366	322	252
2200	3532	2447	1351	1139	904	785	664
4700	7275	4708	2802	2277	1920	1663	1286
10000	16640	10700	6372	5176	4425	3868	3098

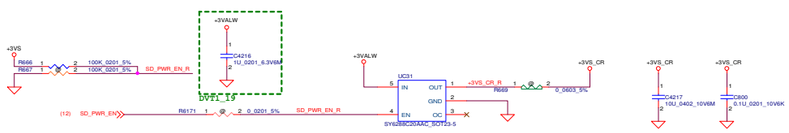
SSD_PWR_2(GEN 2)



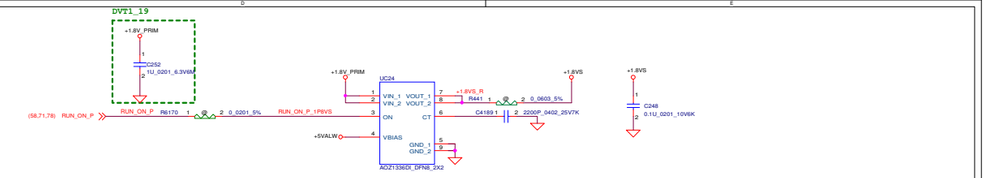
CAMERA



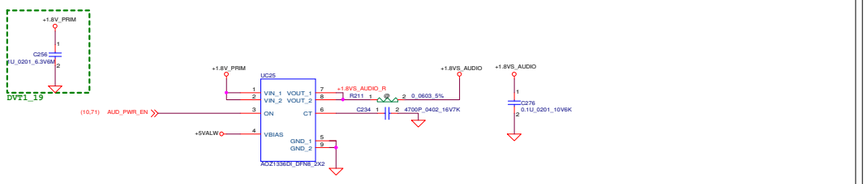
Card Reader



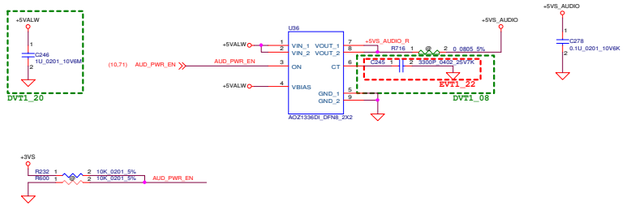
1.8VS



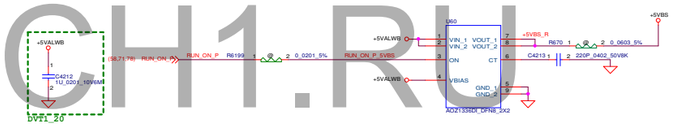
1.8VS_AUDIO



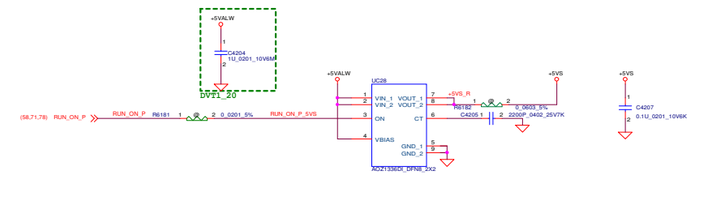
5VS_AUDIO



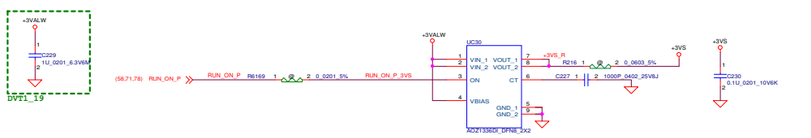
5VBS



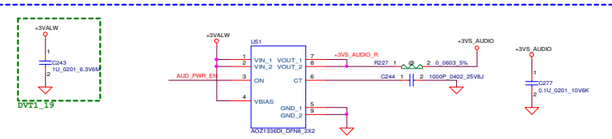
5VS



3VS



3VS_AUDIO



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Title	P071 - DC/DC		
Size	Document Number		Rev
	LA-G172P		1.0 (ADS)
Date:	Friday, May 24, 2019	Sheet 71 of 101	

Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.		
Title	***P072 - Reserve***	
Size	Document Number ***LA-G172P***	Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 72 of 101	

To LEFT Type-C Connector

SW_TBT_L_USB20_P1 1
SW_TBT_L_USB20_N1 2
SW_TBT_L_USB20_P2 3
SW_TBT_L_USB20_N2 4

A_IN
B_IN
USB/I2C MUX_L
B0_OUT
A0_OUT

8 USB20_P8
9 USB20_N8
To PCH & PD_L

17 UPD_L_SMBDAT
18 UPD_L_SMBCLK
0-ohm
0-ohm

To RIGHT Type-C Connector

SW_TBT_R_USB20_P1 1
SW_TBT_R_USB20_N1 2
SW_TBT_R_USB20_P2 4
SW_TBT_R_USB20_N2 3

A_IN
B_IN
USB/I2C MUX_R
B0_OUT
A0_OUT

8 USB20_P9
9 USB20_N9
To PCH & PD_R

17 UPD_R_SMBDAT
18 UPD_R_SMBCLK
0-ohm
0-ohm

0-ohm
+3VALW
G
NC
D
S
0-ohm
+3VALW
G
NC
D
S

+3VALW
2.2K-ohm
2.2K-ohm
UPD_SMBDAT B4
UPD_SMBCLK C3

+3VALW
100K-ohm
100K-ohm

GPIO225
SMB04 EC
GPIO214
F10 UPD_L_SMBINT#
F5 UPD_R_SMBINT#

+VCC3V3_TBT_L_LDO
10K-ohm
10K-ohm
10K-ohm

NC 0-ohm
NC 0-ohm
I2C3_PD_L_CLK_R
I2C3_PD_L_DAT_R
I2C3_PD_L_INT#_R
0-ohm NC
0-ohm NC
0-ohm NC

I2C3_PD_L_INT# 23
I2C3_PD_L_DAT 22
I2C3_PD_L_CLK 21

PD I2C3 for TGL use

SML1_SMBDATA
SML1_SMBCLK
0-ohm
I2C_RT_L_SDA E7
I2C_RT_L_SCL C9
I2C
BB_L
SMB
I2C_INT#
TBT_L_SMBDAT B7
TBT_L_SMBCLK A7
A10 I2C_RT_L_INT#
NC 0-ohm
0-ohm

UPD_SMBDAT_Q
UPD_SMBCLK_Q
SML1_SMBDATA
SML1_SMBCLK
0-ohm
I2C1_PD_L_DAT 28
I2C1_PD_L_CLK 27
I2C2_PD_L_DAT 33
I2C2_PD_L_CLK 32
I2C3_INT#
I2C3
I2C1
I2C1_INT#
PD_L
I2C2
I2C2_INT#
29 I2C1_PD_L_INT# 0-ohm
34 I2C2_PD_L_INT# 0-ohm

+3V_PRIM
1K-ohm
1K-ohm
NC 0-ohm
NC 0-ohm

DL22 SML1_SMBDATA_R
DN22 SML1_SMBCLK_R
SML1
0-ohm
0-ohm

I2C_RT_R_SDA E7
I2C_RT_R_SCL C9
I2C
BB_R
SMB
I2C_INT#
TBT_R_SMBDAT B7
TBT_R_SMBCLK A7
A10 I2C_RT_R_INT#
0-ohm
NC 0-ohm

UPD_SMBDAT_Q
UPD_SMBCLK_Q
SML1_SMBDATA
SML1_SMBCLK
0-ohm
I2C1_PD_R_DAT 28
I2C1_PD_R_CLK 27
I2C2_PD_R_DAT 33
I2C2_PD_R_CLK 32
I2C1
I2C1_INT#
PD_R
I2C2
I2C3_INT#
I2C2_INT#
I2C3
29 I2C1_PD_R_INT# 0-ohm
34 I2C2_PD_R_INT# 0-ohm

+3V_PRIM
499-ohm
499-ohm

DJ24 SML0_SMBDATA
DK24 SML0_SMBCLK
SML0

PCH

100K-ohm
100K-ohm
100K-ohm
100K-ohm

100K PD for non-Vpro use

NC 0-ohm

+VCC3V3_TBT_R_LDO
10K-ohm
10K-ohm
10K-ohm

I2C3_PD_R_INT#_R
I2C3_PD_R_DAT_R
I2C3_PD_R_CLK_R
0-ohm NC
0-ohm NC
0-ohm NC

I2C3_PD_R_INT# 23
I2C3_PD_R_DAT 22
I2C3_PD_R_CLK 21

PD I2C3 for TGL use

NC 0-ohm
NC 0-ohm

+3V_PRIM
10K-ohm

CL39 GPP_B11
0-ohm
TBT_I2C_INT#

GPP_B11

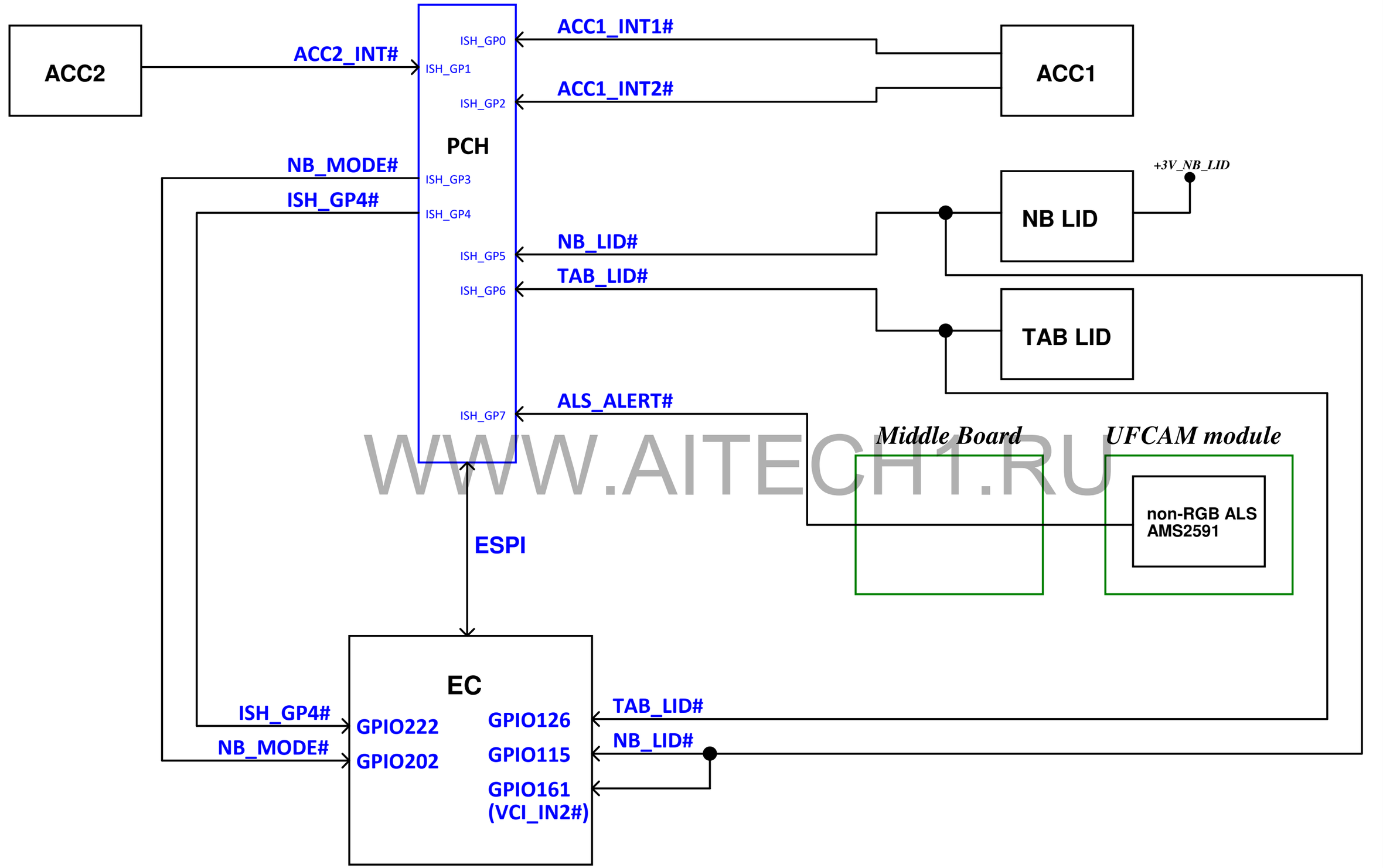
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.

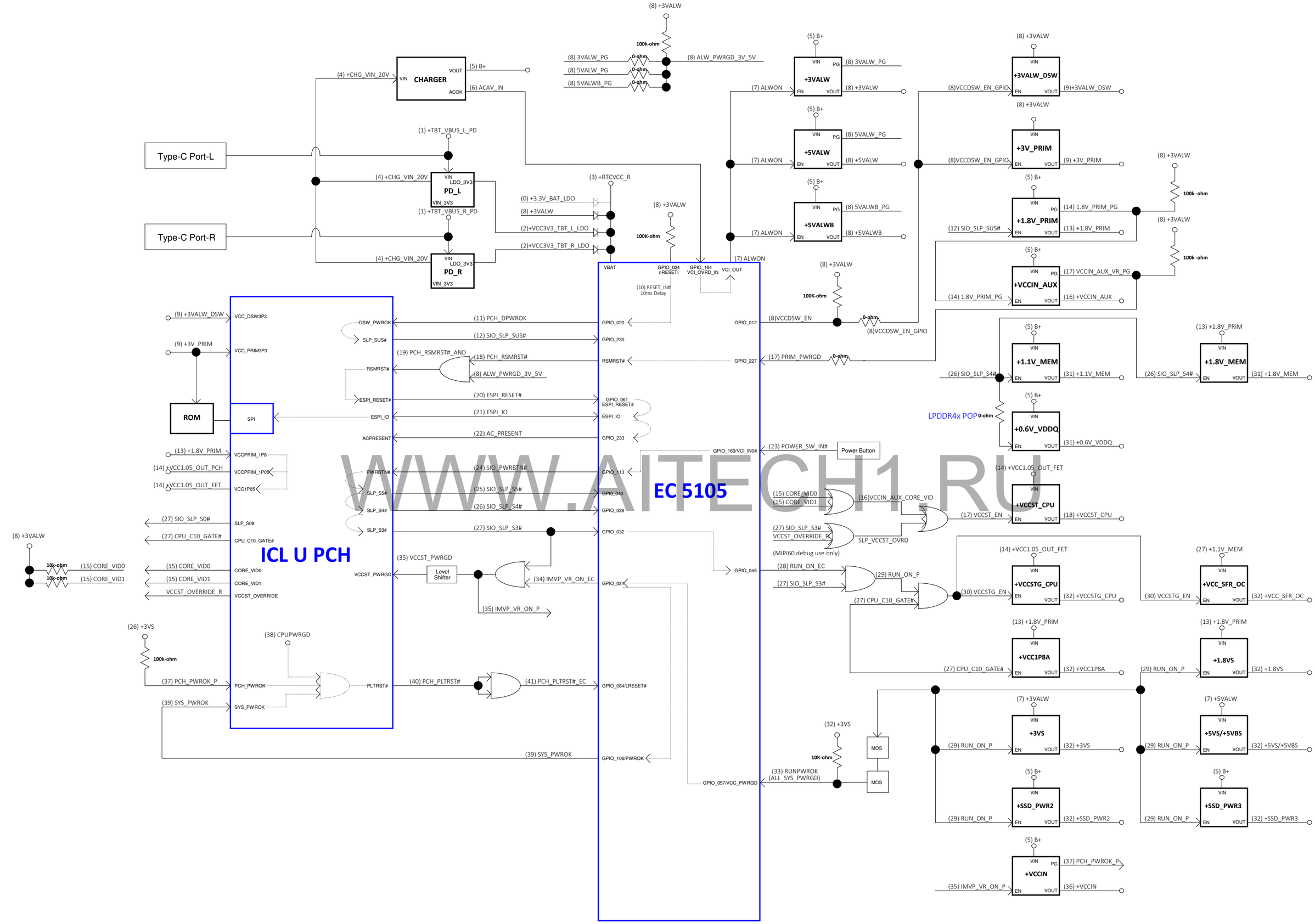
Title: P073 -TBT I2C/SML block diagram

Size	Document Number	Rev
	LA-G172P	1.0 (A00)

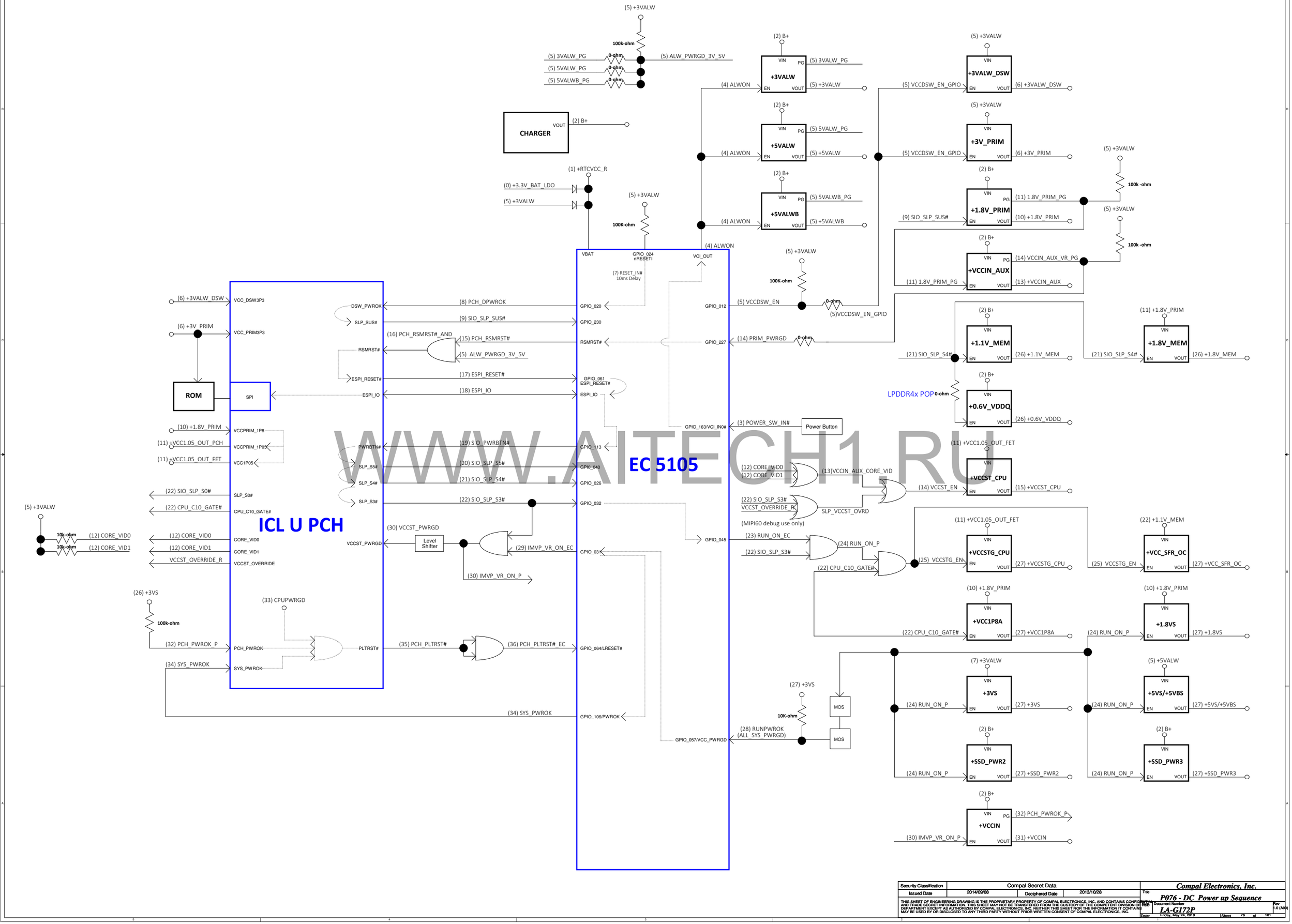
Date: Friday, May 24, 2019 Sheet 73 of 101



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date 2013/10/28	Title: P074 - Sensor block diagram
			Size / Document Number: LA-G171P / Rev: 1.0 (A00)
			Date: Friday, May 24, 2019 / Sheet 74 of 101



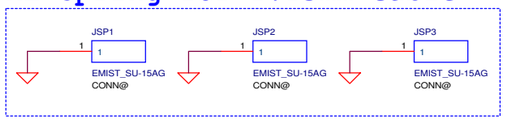
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28
Title	P075 - AC_Power up Sequence		
Document Number	LA-G172P		Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 75 of 101		



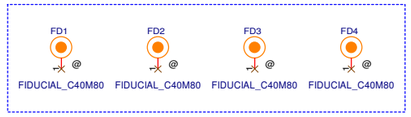
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/09/08	Deciphered Date	2013/10/28
Title	P076 - DC_Power up Sequence		
Document Number	LA-G172P		Rev 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 76 of 101		

Screw Hole

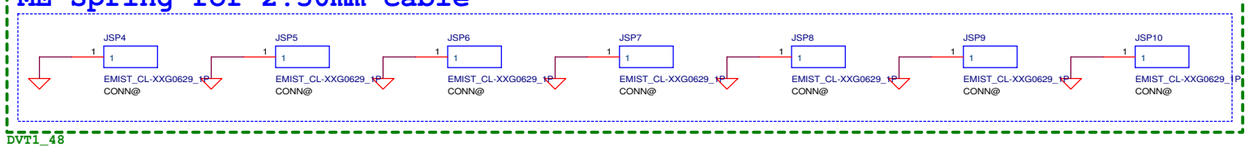
ME Spring for 1.13mm cable



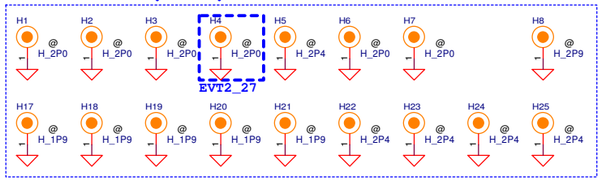
Fiducial Mark



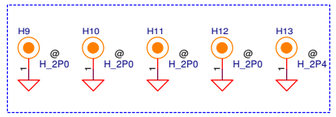
ME Spring for 2.50mm cable



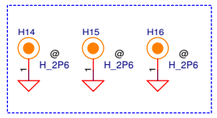
PCB X 17(PTH)



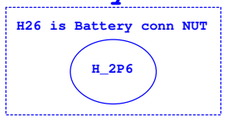
CPU X 5



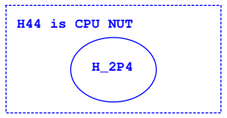
RF X 3



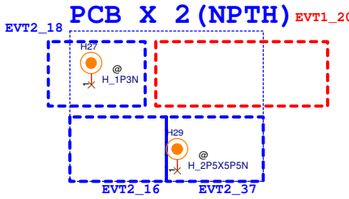
Battery X 1



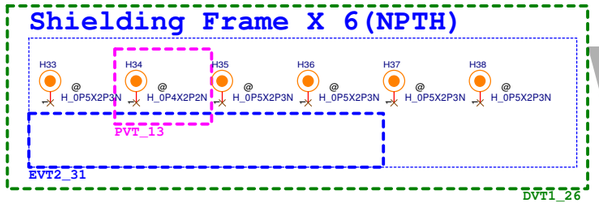
CPU X 1



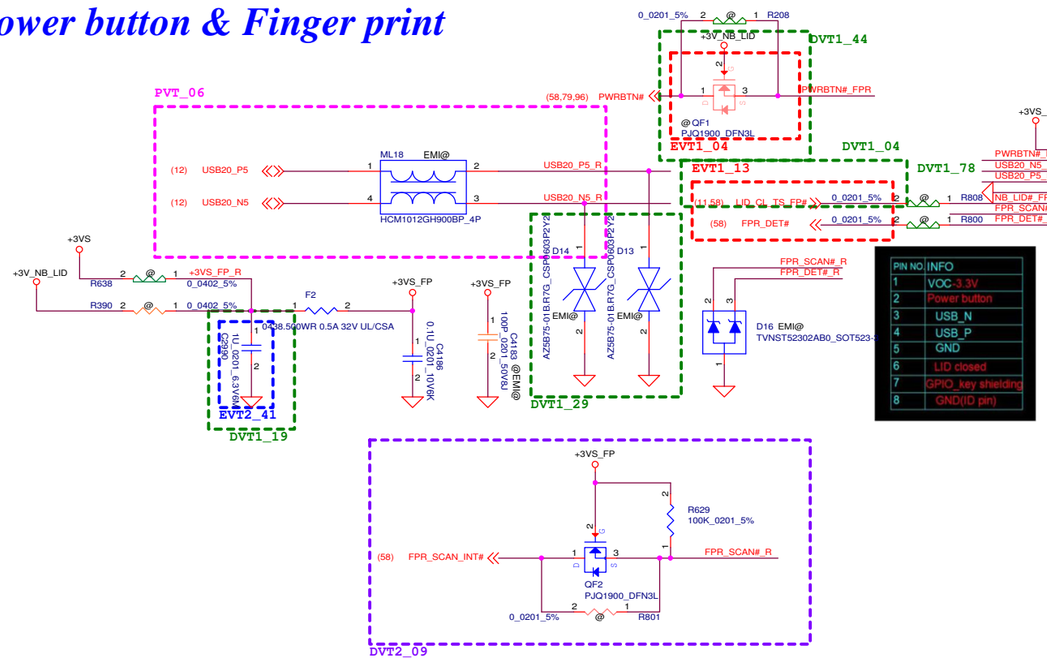
PCB X 2(NPTH)



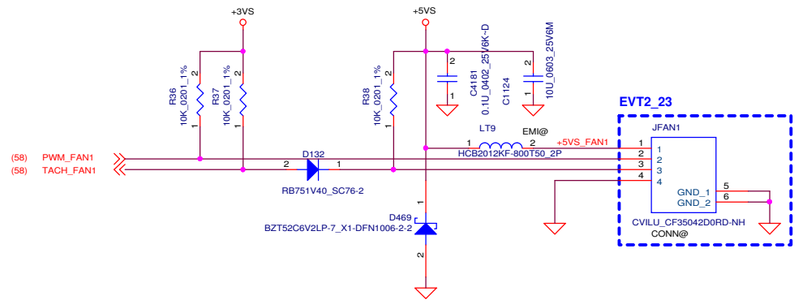
Shielding Frame X 6(NPTH)



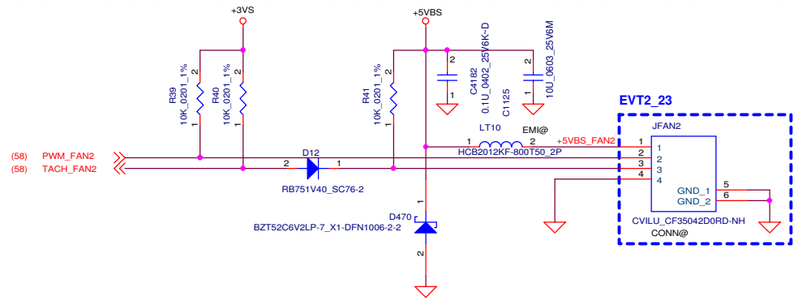
Power button & Finger print



FAN1



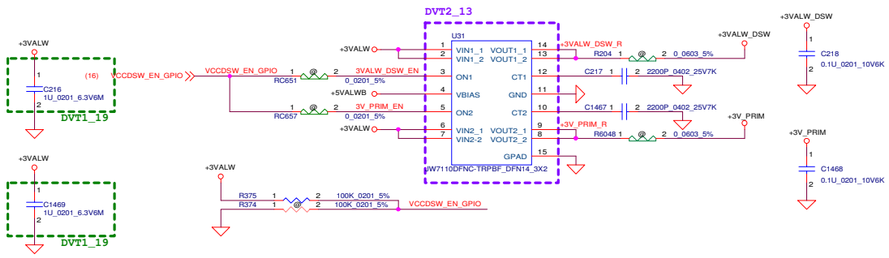
FAN2



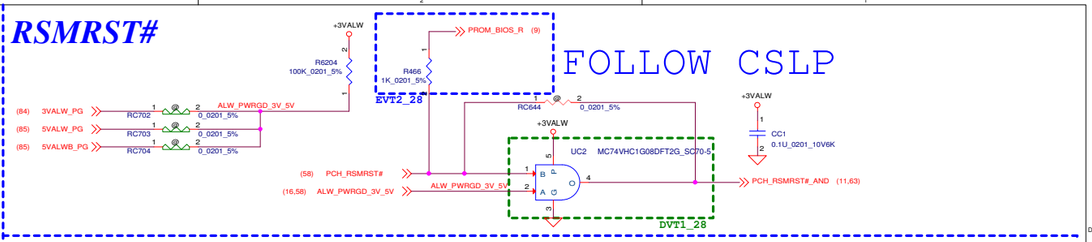
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P077 - PWRBTN&FPR/SCREW/FAN		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
Date:	Friday, May 24, 2019	Sheet 77 of 101	

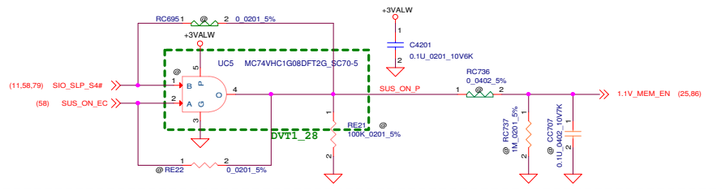
+3VALW_DSW&+3V_PRIM



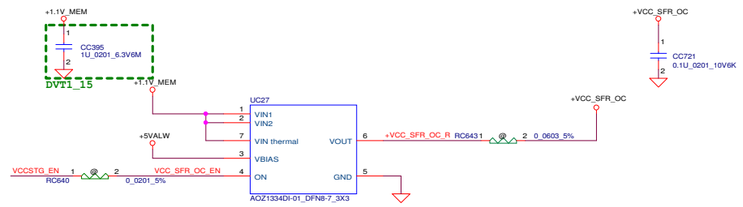
RSMRST#



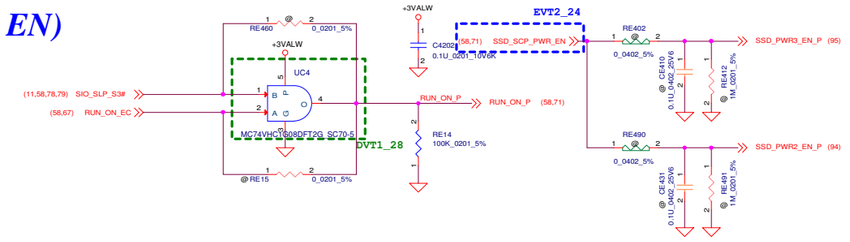
SUS_ON(DDR EN)



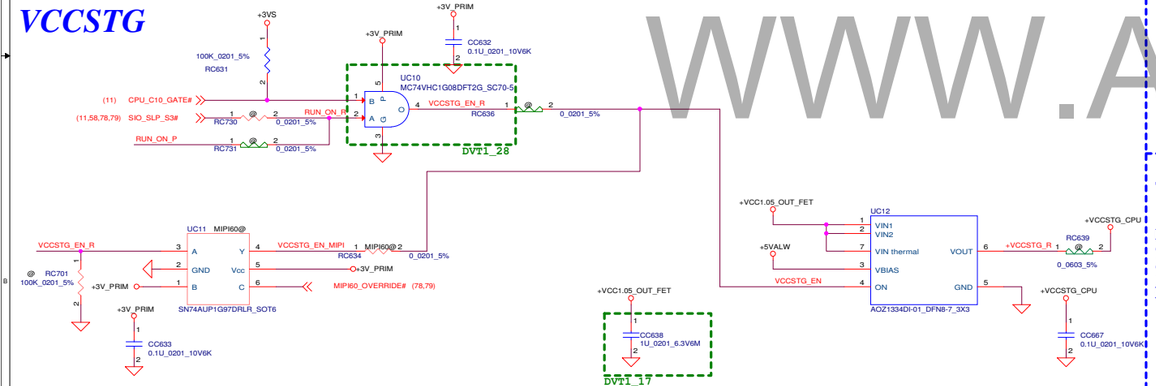
VCC_SFR_OC(VCCPLL_OC)



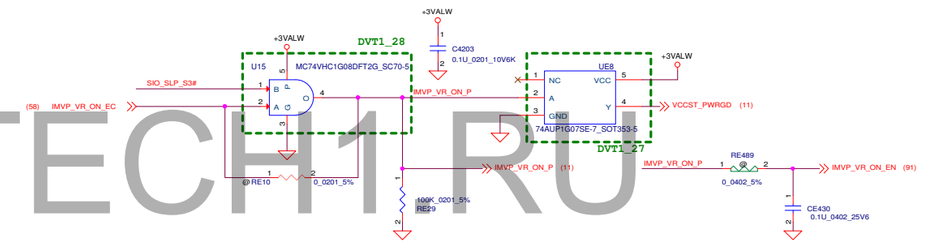
RUN_ON(VS EN)



VCCSTG



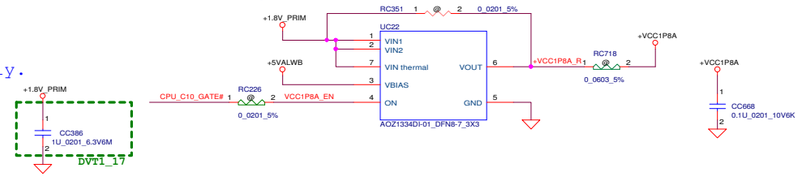
IMVP_VR_ON&VCCST_PWRGD



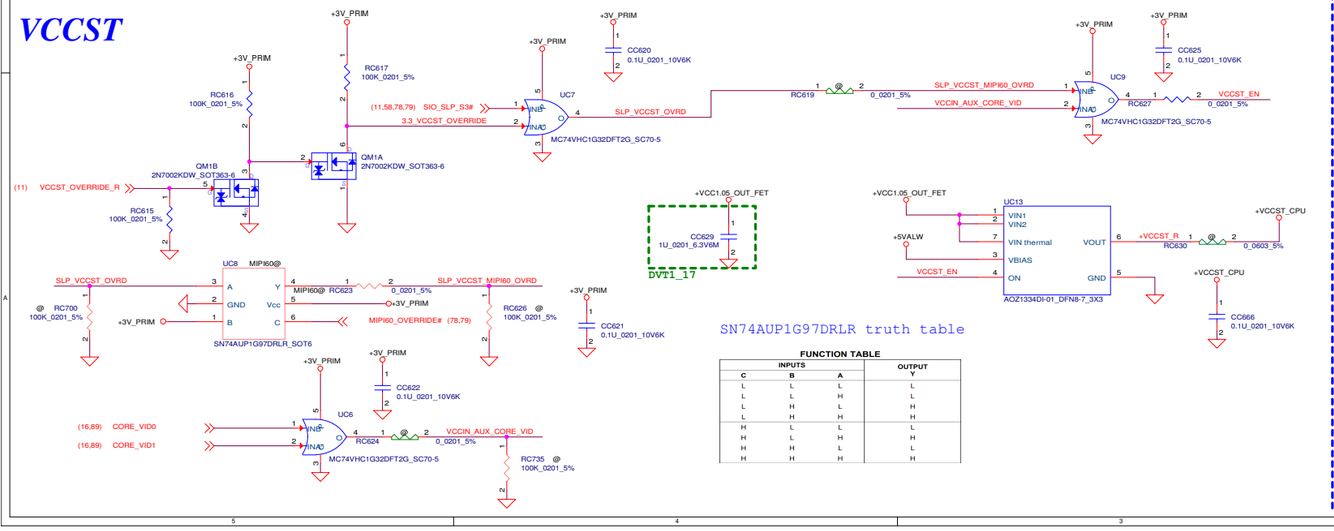
+VCC1P8A

PDG p.615
TCSS and AGSH
Type C Sub system and
processor analog supply.

VCC1P8A shape from VR to VCC1P8A pins should have:
a. total length L of < 22mm between VR and BGA.
b. Average width W of 1.8mm.



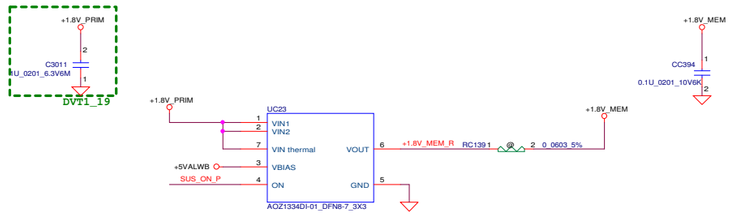
VCCST



SN74AUP1G97DRLR truth table

FUNCTION TABLE			
INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

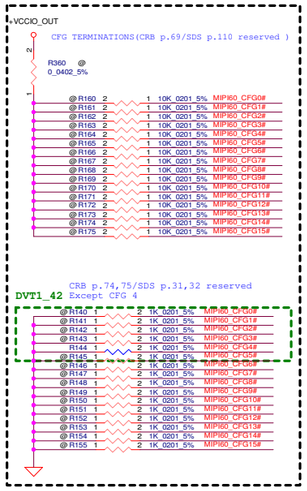
+1.8_MEM

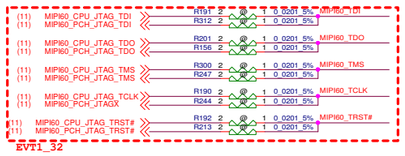


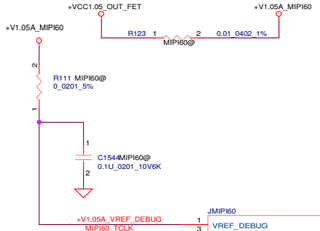
Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

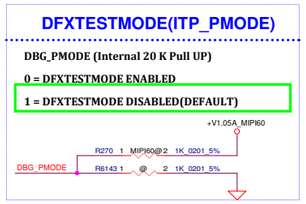
Compal Electronics, Inc.			
Title	P078 - DC/DC & Sequence Logic		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
Date:	Friday, May 24, 2019	Sheet 78 of 101	

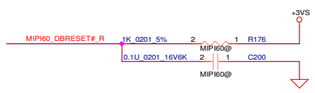
MIPI 60

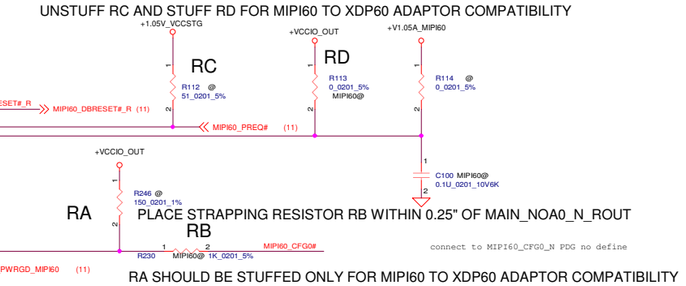


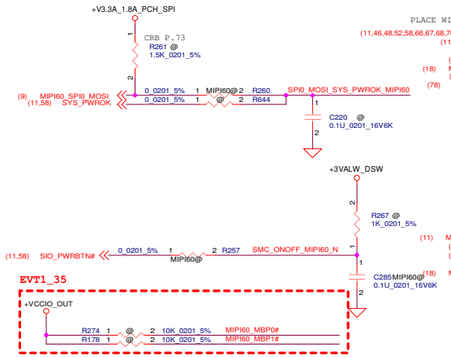


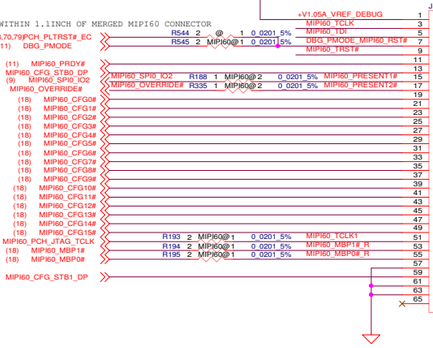


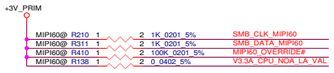


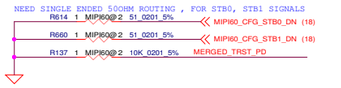






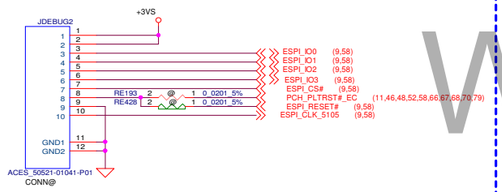




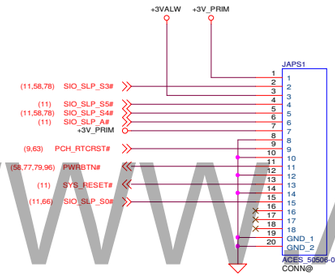


JESPI

LPC &Port Debug	LPC	ESPI
1	+3VS	+3VS
2	+3VS	+3VS
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLK	ESPI_CLK

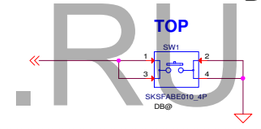


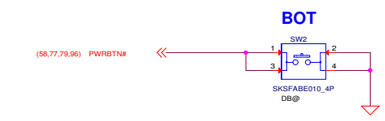
APS



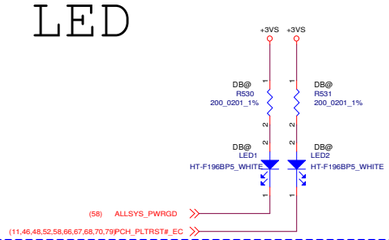
BIOS UART Debug

Power Button Debug

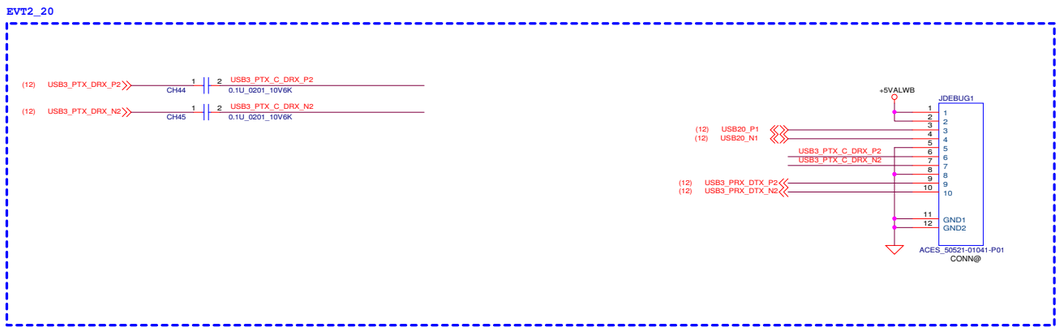




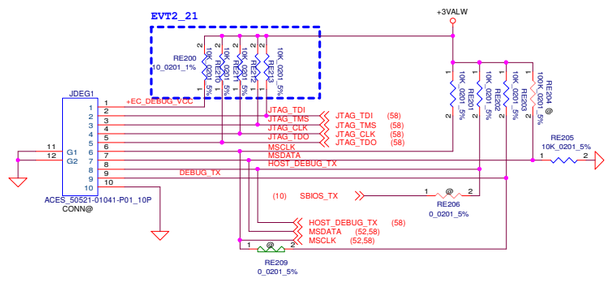
Debug LED



DCI Debug

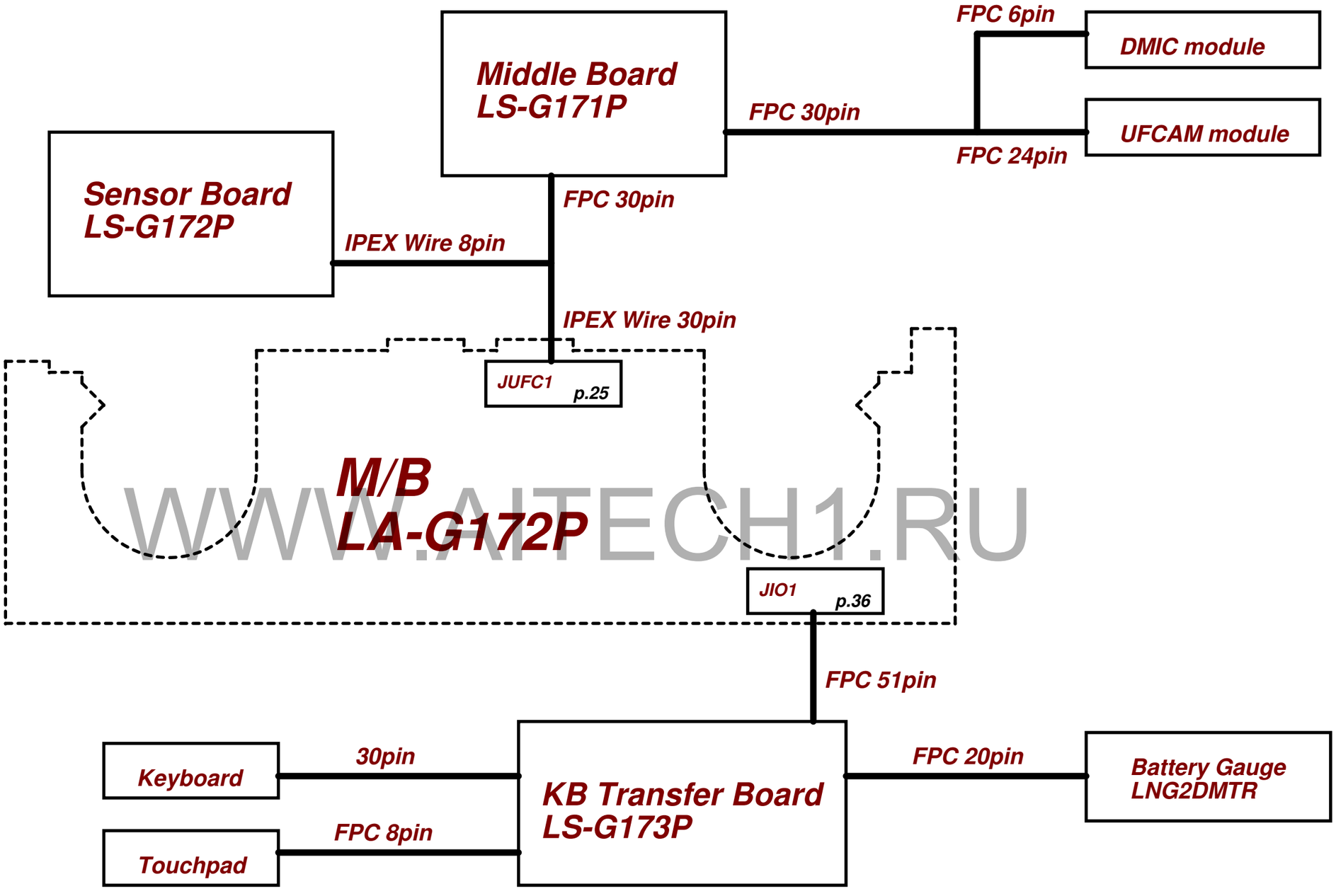


JDEG1
EC UART Debug/80 port



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P079 - Debug APS,DEG,eSPI,LED		
Size	Document Number		Rev
	LA-G172P		1.0 (A00)
Date:	Friday, May 24, 2019	Sheet	79 of 101



Security Classification	Compal Secret Data		
Issued Date	2014/09/08	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P080 - DaughterB Block Diagram			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 80 of 101		

Centenario POWER BLOCK DIAGRAM

Power Rail

Power Trace

Type-C Port-L

Type-C Port-R

PD1 Controller TPS65987DJ

EC MEC5105

PD2 Controller TPS65987DJ

2S2P Battery 51W

Buck-boost Charger ISL9538B (NVDC) Page:83

B+

B+

B+

B+

B+

ALWON_3VALW

+3.3VALW
TDC: 5.1A
Peak Current 7.22A
(NB502)
Page:84

ALWON_5VALW

+5VALW
TDC 5A
Peak Current 7.2A
(NB502)
Page:85

ALWON_5VALWB

+5VALWB
TDC 3.5A
Peak Current 5A
(NB502)
Page:85

IMVP_VR_ON_EN

VCCIN
TDC 36A
Peak Current 70A
(MP2940A)
Page:91,92,93

1.8V_PRIM_PG

VCCIN_AUX
TDC 10A
Peak Current 32A
(MP2941)
Page:89,90

1.1V_MEM_EN

+1.1V_MEM
TDC 4A
Peak Current 5.7A
(RT6243B)
Page:86

0.6V_VDDQ_EN_P

+0.6V_VDDQ (LPDDR4X only)
TDC 1.25A
Peak Current 1.79A
(NB691)
Page:87

PCH_PRIM_EN

+1.8VPRIM
TDC 2.56A
Peak Current 3.65A
(NB691)
Page:88

SSD_PWR2_EN_P

+SSD_PWR2
TDC 1.4A
Peak Current 2A
(NB691)
Page:94

SSD_PWR3_EN_P

+SSD_PWR3
TDC 1.4A
Peak Current 2A
(NB693)
Page:95

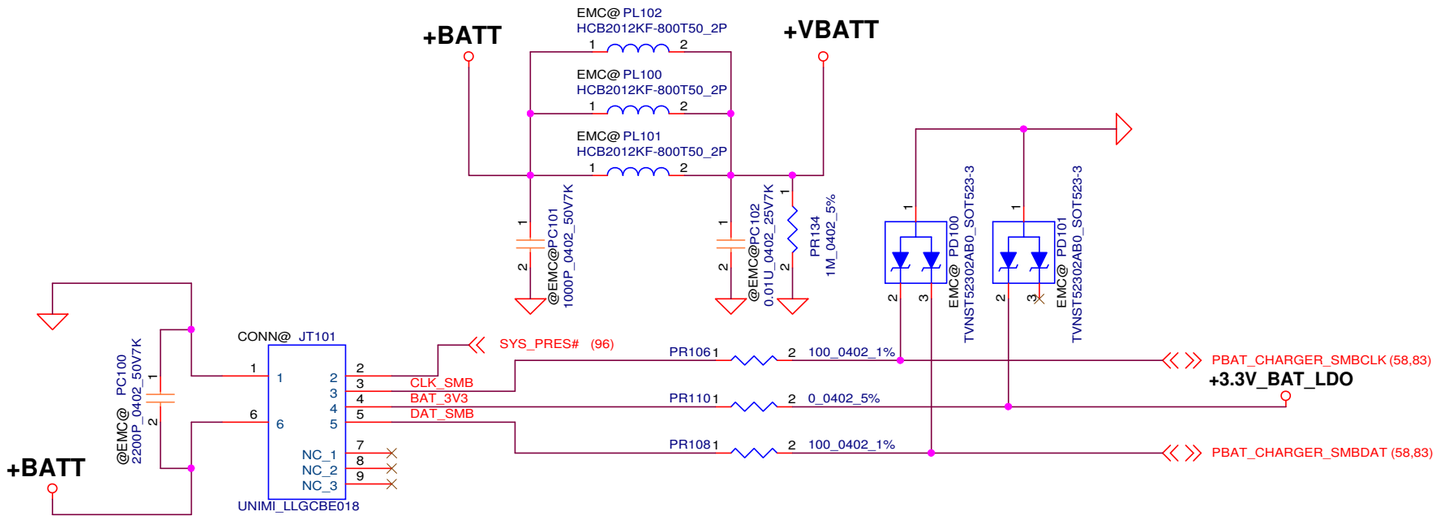
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

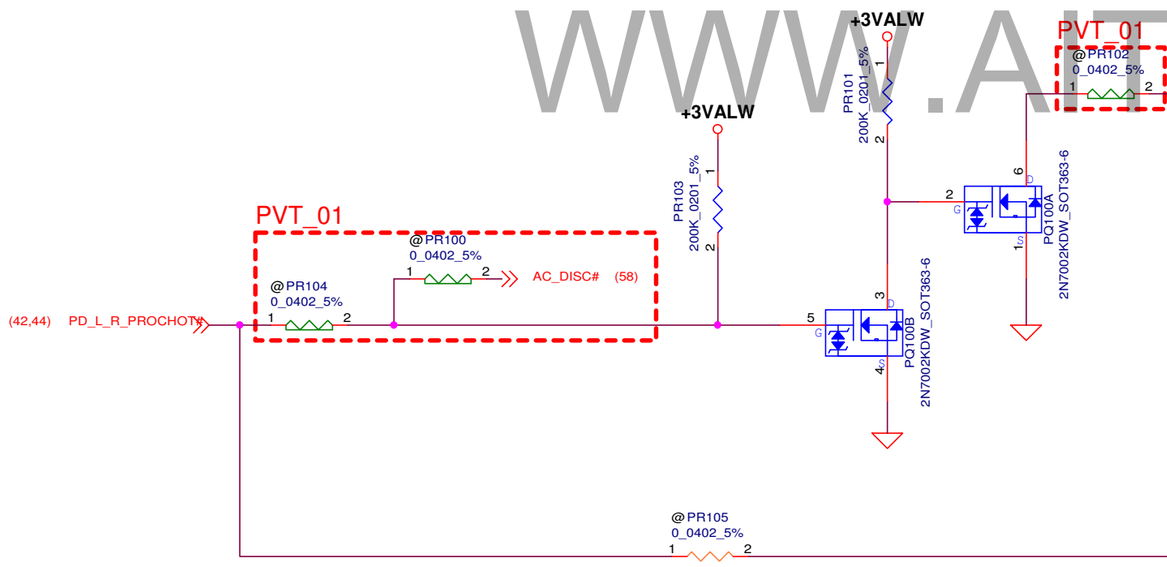
Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Size | Document Number: LA-G172P | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 81 of 101

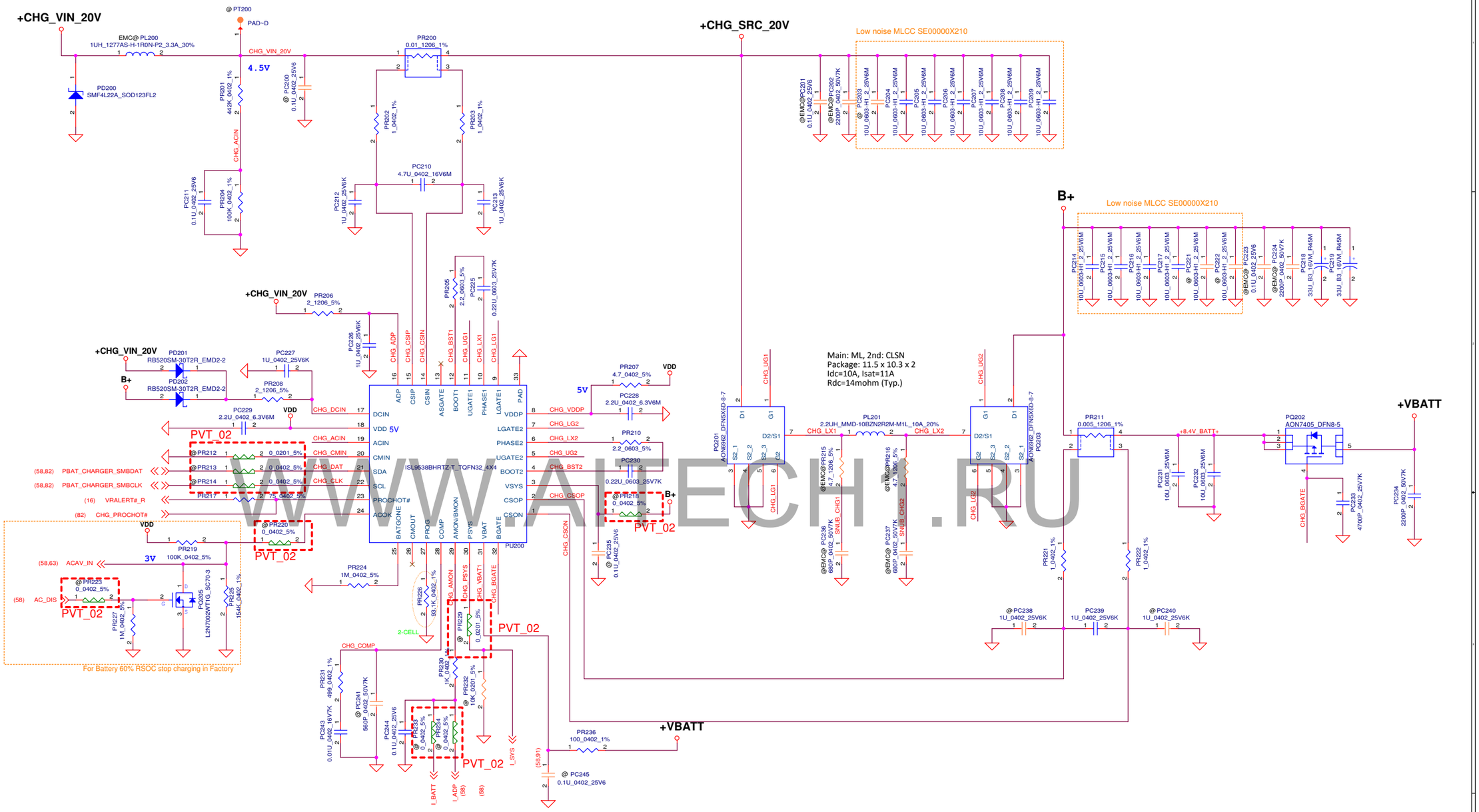




Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title: PWR DCIN			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 82 of 101		

Charger controller(40.1), Support component(40.2)



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.	
Title	PWR_Charger
Size	Document Number: LA-G172P
Rev	1.0 (A00)
Date:	Friday, May 24, 2019
Sheet	83 of 101

3VALW
TDC 5.05A
Peak Current 7.22A
OCP 10A
700kHz

VCC	MODE2 Set
INT VCC	0
EXT VCC	Connect to VIN

CLM	Resistor to GND
7A	0
10A	90K
13A	150K
16.5A	>230K or float

Main: CLSN, 2nd:
Package: 7.3 x 6.8 x 1.5
Idc=6.5A, Isat=12A
DCR=20mohm (Typ.)

B+
EMC@ PL302 HCB2012KF-800T50_2P
EMC@ PL300 HCB2012KF-800T50_2P
@EMC@ PC301 0.1U_0402_25V6
@EMC@ PC302 220P_0402_50V7K
PC303 10U_0603_25V6M
PC304 10U_0603_25V6M
@PR300 0_0402_5%
PVT_03
PR301 90.9K_0201_1%
PR303 0_0603_5%
PC300 0.22U_0402_16V7K
BST_3V
PU300
VIN
MODE2
CLM
BST
SW
LX_3V
PL301 1.5UH_MHCB06015-1R5M-C1_6.5A_20%
+3VALWP
R4
PR306 768K_0402_1%
PC305 220P_0201_25V7K
PR304 26.1K_0402_1%
R1
PR307 499_0402_1%
PR309 30.1K_0402_1%
R2
PC306 22U_0603_6.3V6M
PC307 22U_0603_6.3V6M
PC308 22U_0603_6.3V6M
PC309 22U_0603_6.3V6M
PC310 22U_0603_6.3V6M
PC311 22U_0603_6.3V6M
(58,96) ALWON_3VALW
EN
FB
FB_3V
(78) 3VALW_PG
PG
NB502GQ-Z_QFN16_3X3
@PR308 150K_0201_5%
+3.3V_ALW2
3V3 3.6V
PGND
GND_1
GND_2
GND_3
GND_4
MODE1
NC
PC313 2.2U_0402_6.3V6M
@PR310 0_0402_5%
@EMC@ PR311 4.7_0805_5%
@EMC@ PC314 680P_0603_50V7K

State	VOUT	Fs	Resistor to GND
M1	Vo<3V	700kHz	0
M2	Vo<3V	1000kHz	90K
M3	Vo>=3V	1000kHz	150K
M4	Vo>=3V	700kHz	>230K or float

MODE	VREF
Vo<3V	0.6V
Vo>3V	1.8V

$$R1 = \frac{1}{\frac{VREF}{VOUT-VREF} - \frac{R2}{R4}} \times R2$$

+3VALWP
@PJP300
JUMP_43X118
+3VALW

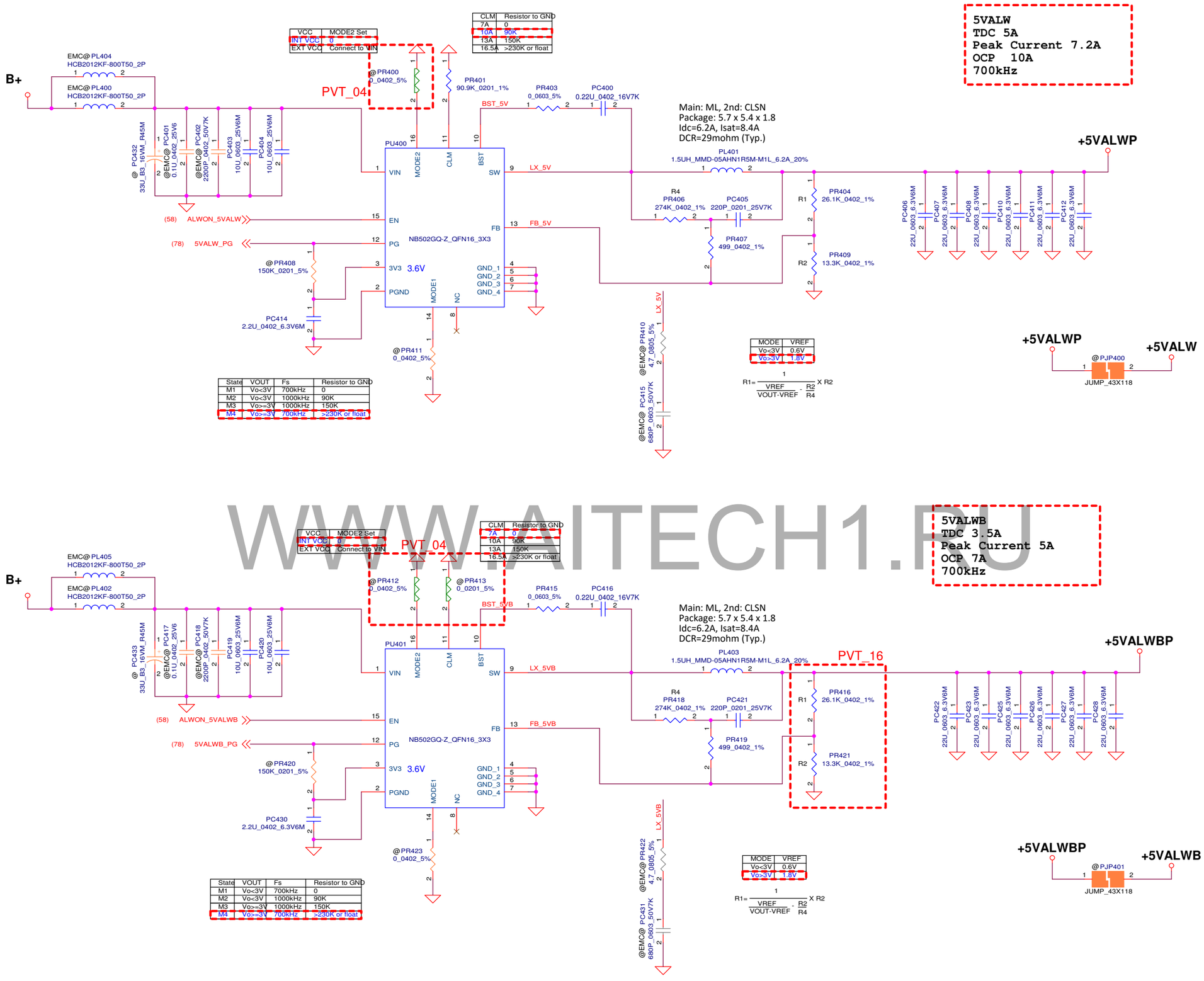
Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: ***PWR_+3VALW***

Size | Document Number: ***LA-G172P*** | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 84 of 101



VCC	MODE2 Set
INT VCC	0
EXT VCC	Connect to VIN

CLM	Resistor to GND
7A	0
10A	90K
13A	150K
16.5A	>230K or float

State	VOUT	Fs	Resistor to GND
M1	Vo<3V	700kHz	0
M2	Vo<3V	1000kHz	90K
M3	Vo>=3V	1000kHz	150K
M4	Vo>=3V	700kHz	>230K or float

MODE	VREF
Vo<3V	0.6V
Vo>3V	1.8V

$$R1 = \frac{1}{\frac{VREF}{VOUT-VREF} - \frac{R2}{R4}} \times R2$$

VCC	MODE2 Set
INT VCC	0
EXT VCC	Connect to VIN

CLM	Resistor to GND
7A	0
10A	90K
13A	150K
16.5A	>230K or float

State	VOUT	Fs	Resistor to GND
M1	Vo<3V	700kHz	0
M2	Vo<3V	1000kHz	90K
M3	Vo>=3V	1000kHz	150K
M4	Vo>=3V	700kHz	>230K or float

MODE	VREF
Vo<3V	0.6V
Vo>3V	1.8V

$$R1 = \frac{1}{\frac{VREF}{VOUT-VREF} - \frac{R2}{R4}} \times R2$$

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.	
Title	PWR_+5VALW/+5VALWB
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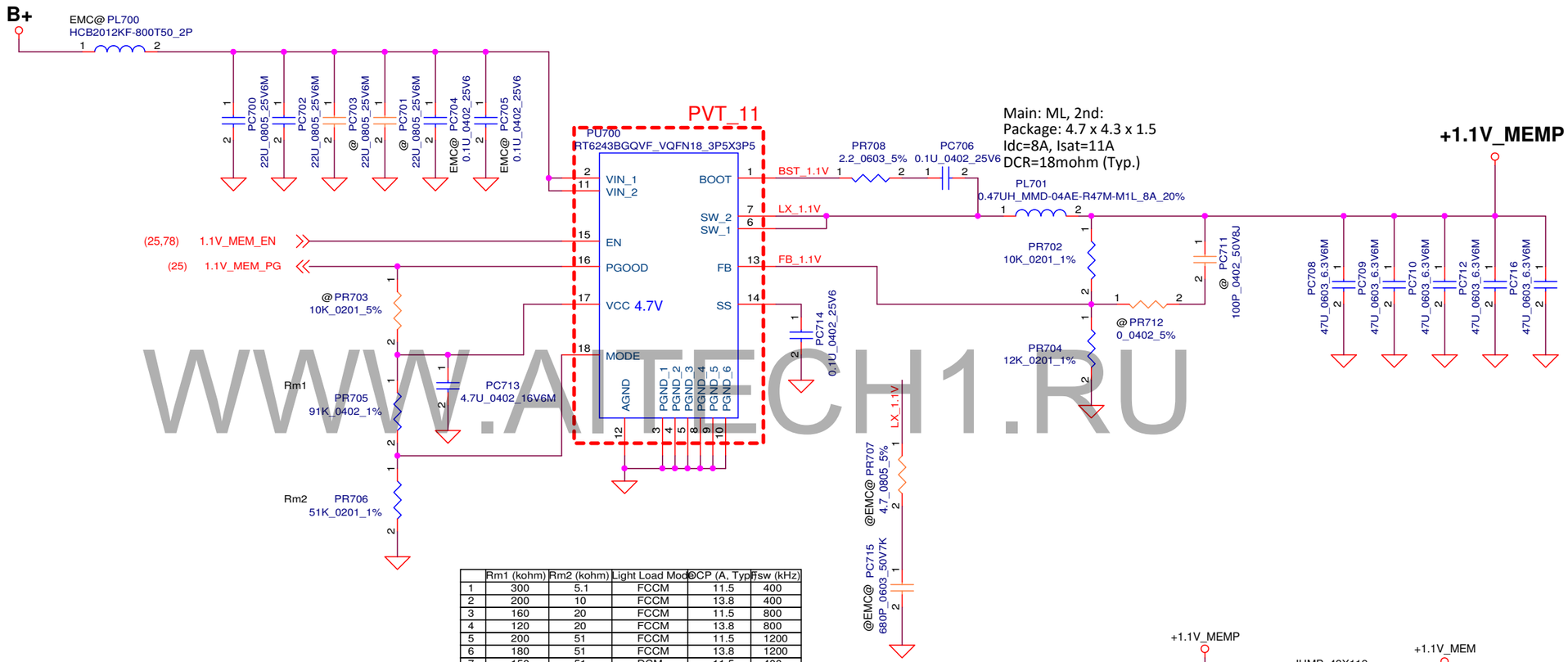
1.1V_MEM
TDC 4A
Peak Current 5.7A
OCP 11.5A
800KHz



	Rm1 (kohm)	Rm2 (kohm)	Light Load Mode	OCP (A, Typ)	fsw (kHz)
1	300	5.1	FCCM	11.5	400
2	200	10	FCCM	13.8	400
3	160	20	FCCM	11.5	800
4	120	20	FCCM	13.8	800
5	200	51	FCCM	11.5	1200
6	180	51	FCCM	13.8	1200
7	150	51	DCM	11.5	400
8	120	51	DCM	13.8	400
9	91	51	DCM	11.5	800
10	82	51	DCM	13.8	800
11	62	51	DCM	11.5	1200
12	51	51	DCM	13.8	1200

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

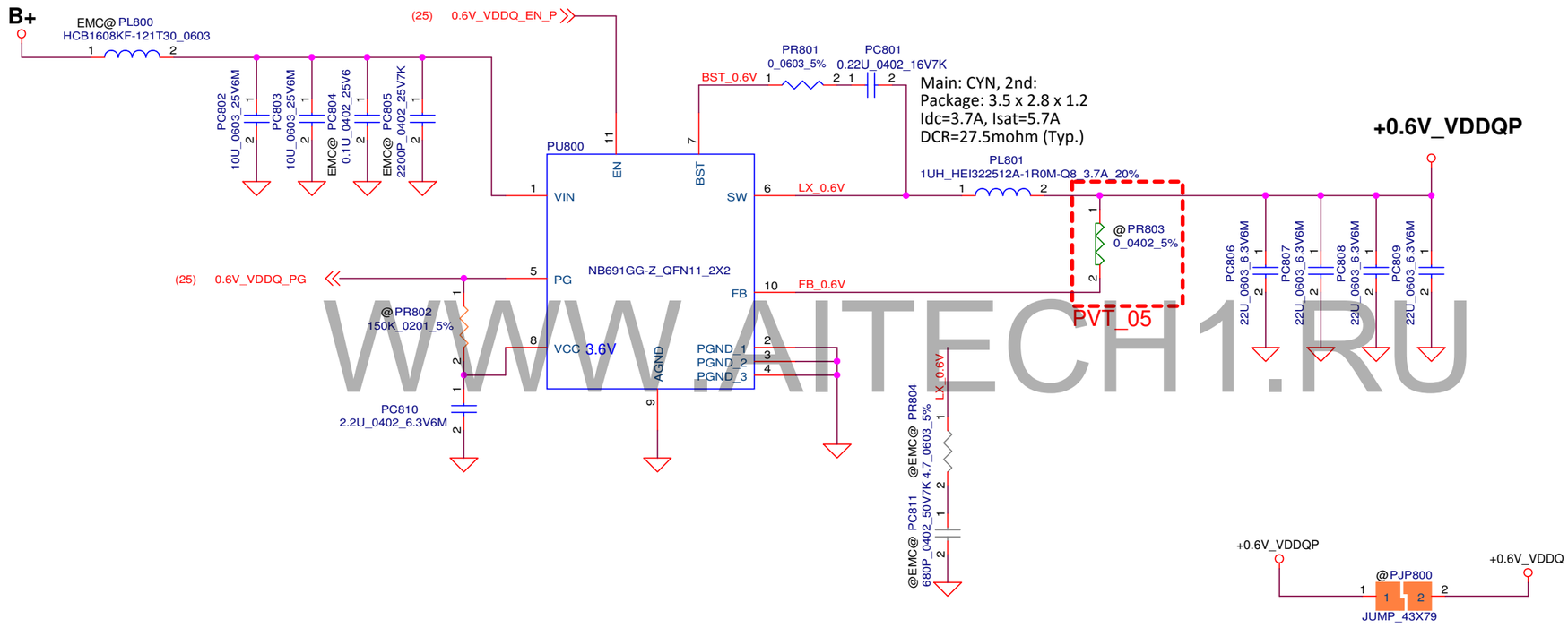
Compal Electronics, Inc.

Title: ***PWR_+1.1V_MEM***

Size | Document Number: ***LA-G172P*** | Rev: 1.0 (A00)

Date: Friday, May 24, 2019 | Sheet 86 of 101

0.6V_VDDQ
TDC 1.25A
Peak Current 1.79A
OCP 7.5 (Typ.)
750kHz



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title: PWR_VDDQ4x			
Size	Document Number: LA-G172P		Rev: 1.0 (A00)
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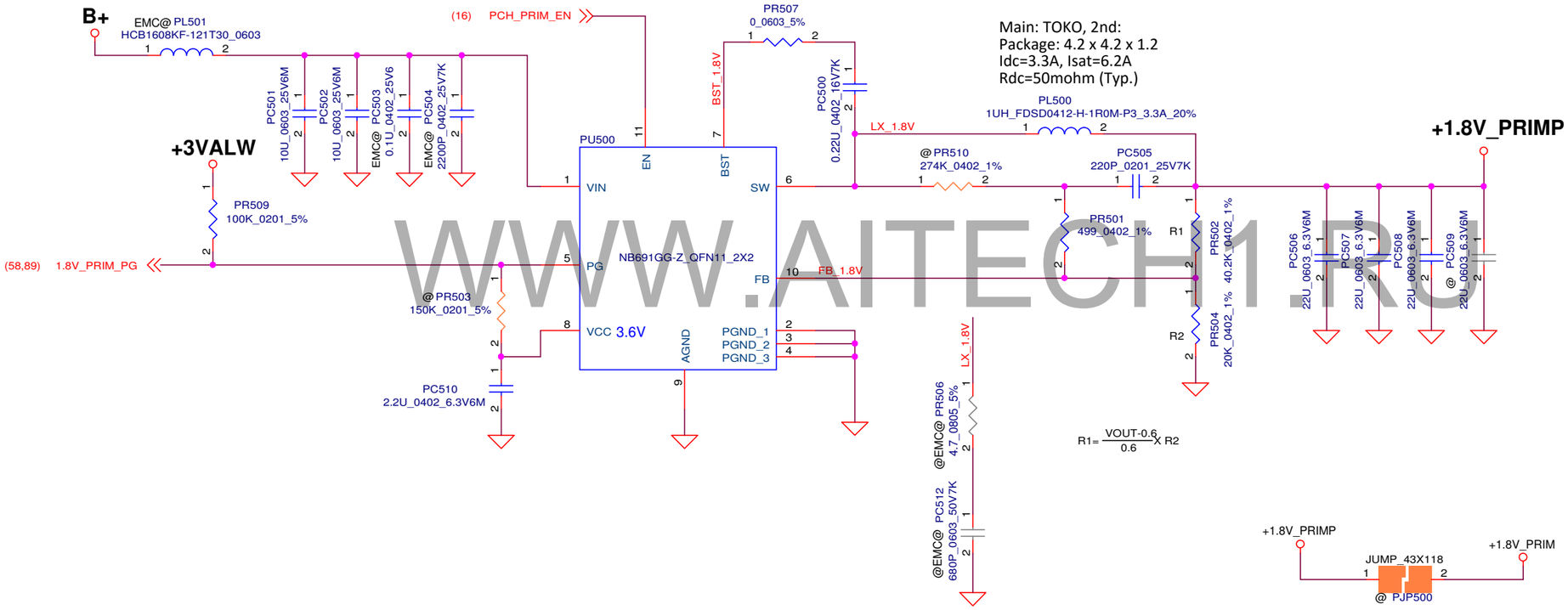
1.8V_PRIM
TDC 2.56A
Peak Current 3.65A
OCP 7.5A (Typ.)
750kHz



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title	PWR_+1.8VPRIM		
Size	Document Number LA-G172P		Rev 1.0 (A00)
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VCCIN_AUX (Base on PDG rev 1.35)
Peak Current 32A (ICCmax)
TDC :14A
OCP Current 32A "valley" current-sensing
Fsw=1MHz

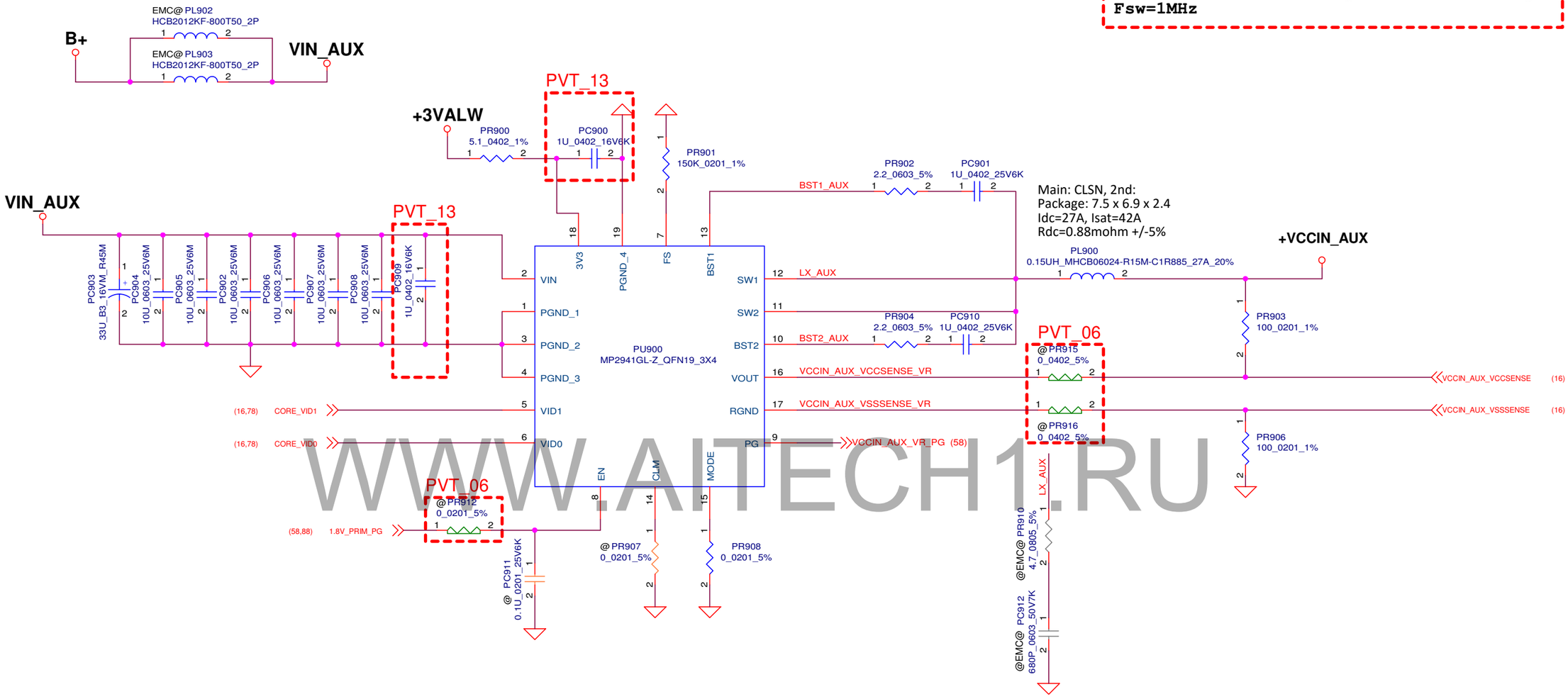

Table---1:VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	16A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

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Compal Electronics, Inc.			
Title: PWR_VCCIN_AUX			
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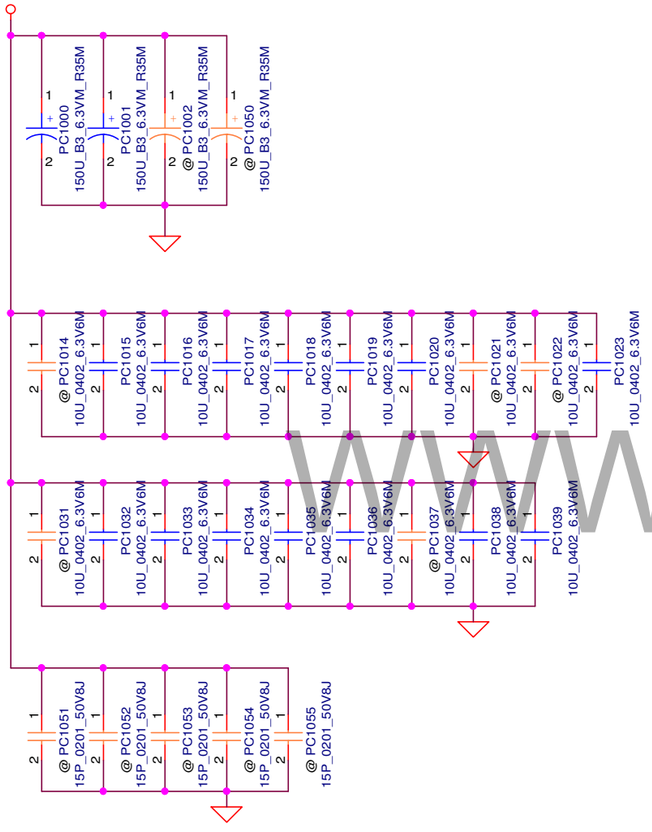
150U_B3 * 4 (POP*2, NC*2)
10U_0402 * 19 (POP*14, NC*5)
22U_0603 * 10 (POP*1, NC*9)
47U_0603 * 7 (POP*1, NC*6)
1U_0201 * 5 (NC*5)
0.1U_0201 * 5 (NC*5)

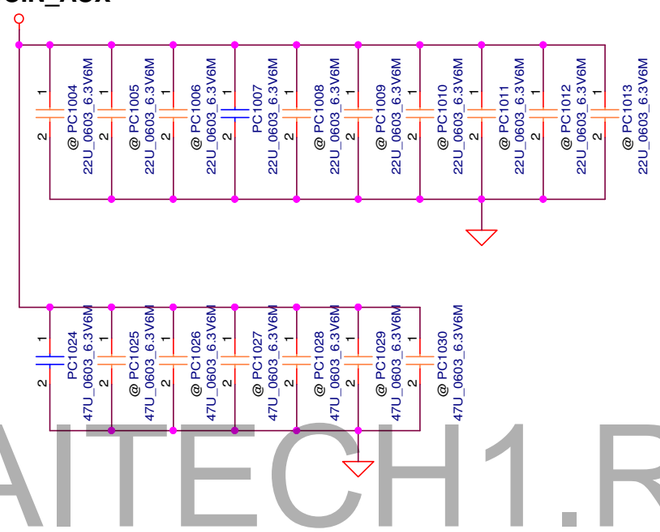
PDG ver 1.35 Primary side:
2x 330uF 7343
3x 22uF 0603
12x 10uF 0402
1x 47uF 0805

Primary side

+VCCIN_AUX



+VCCIN_AUX



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.		
Title: PWR_DECOUPLING-VCCIN_AUX		
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VCCIN (Base on PDG rev 1.35)
Peak Current 70A (ICCmax)
PL2 TDC :39A
DC Load line :2mV/A
AC Load line :4.2mV/A
OCP Current 90A
Fsw=600kHz

(92) VRACPU_VTEMP
PR1101 49.9K_0402_1%
PC1100 2.2U_0402_6.3V6M
+3VALW
PR1102 4.7_0402_5%
PC1101 4.7U_0402_6.3V6M
PVT_07
@PR1103 0_0201_5%
(58,83) I_SYS
CPU_B+ Psys=65+51=116W
PR1100 9.09K_0402_1%
PC1102 1000P_0402_25V8J
PR1104 2M_0402_1%
PWM1 (92)
PWM2 (92)
IMVP_VR_ON_EN (78)
CSSUM
PR1107 1.5K_0402_1%
PR1108 1.5K_0402_1%
PR1106 133K_0402_1%
PC1104 0.1U_0402_25V7K
PU1100
VIN_SEN PSYS TEMP VDD33 PWM1 PWM2 PWM3
3.3V
+3VALW
PR1111 10K_0201_5%
PVT_07
@PR1115 0_0201_5%
+1.05V_VCCSTG +3VALW
@PR1109 10K_0201_5%
@PR1112 10K_0201_5%
@PR1113 10K_0201_5%
@PR1114 1.91K_0402_1%
PVT_07
PVT_07
@PR1110 0_0402_5%
(92) CS2
(92) CS1
+VCCIN
@PR1116 0_0402_5%
@PC1105 390P_0402_50V7K
@PR1120 4.99K_0402_1%
PR1117 806_0402_1%
@PC1103 150P_0402_50V8J
VFB
CS3 CS2 CS1 VDIFF VFB VOSEN VORTN
MP2940AGRT-0010-Z_TQFN28_4X4
EN PE STB SCL_P SDA_P VRHOT# VRRDY
PE
SYNC (92)
IMVP_SMBCLK_VR
IMVP_SMBDAT_VR
PR1123 75_0402_5%
@PR1118 0_0402_5%
@PR1121 0_0402_5%
@PR1125 0_0201_5%
IMVP_SMBCLK (58)
IMVP_SMBDAT (58)
H_PROCHOT# (11,16,58)
PCH_PWROK_P (11)
PR1119 100_0201_1%
(14) VCCIN_SENSE
(14) VSSIN_SENSE
PR1126 100_0201_1%
@PR1122 0_0402_5%
@PR1124 0_0402_5%
PVT_07
VCCIN_SENSE_VR
VSSIN_SENSE_VR
1.8V
CSSUM IMON IREF VDD18 SCLK/VID0 SDIO/VID1 ALT# AGND
+1.05V_VCCST
PC1106 0.1U_0201_25V6K
PR1127 45.3_0402_1%
PR1128 100_0402_1%
PR1129 45.3_0402_1%
SVID_ALERT#_VR
SVID_DAT_VR
SVID_CLK_VR
@PR1130 0_0402_5%
@PR1131 0_0402_5%
@PR1132 0_0402_5%
PVT_07
SVID_ALERT# (14)
SVID_DAT (14)
SVID_CLK (14)
CSSUM
IMON
PR1133 60.4K_0402_1%
PC1107 330P_0402_50V8J
PR1134 61.9K_0402_1%
VDD18
PC1108 2.2U_0402_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: PWR_VCCIN_CTRL

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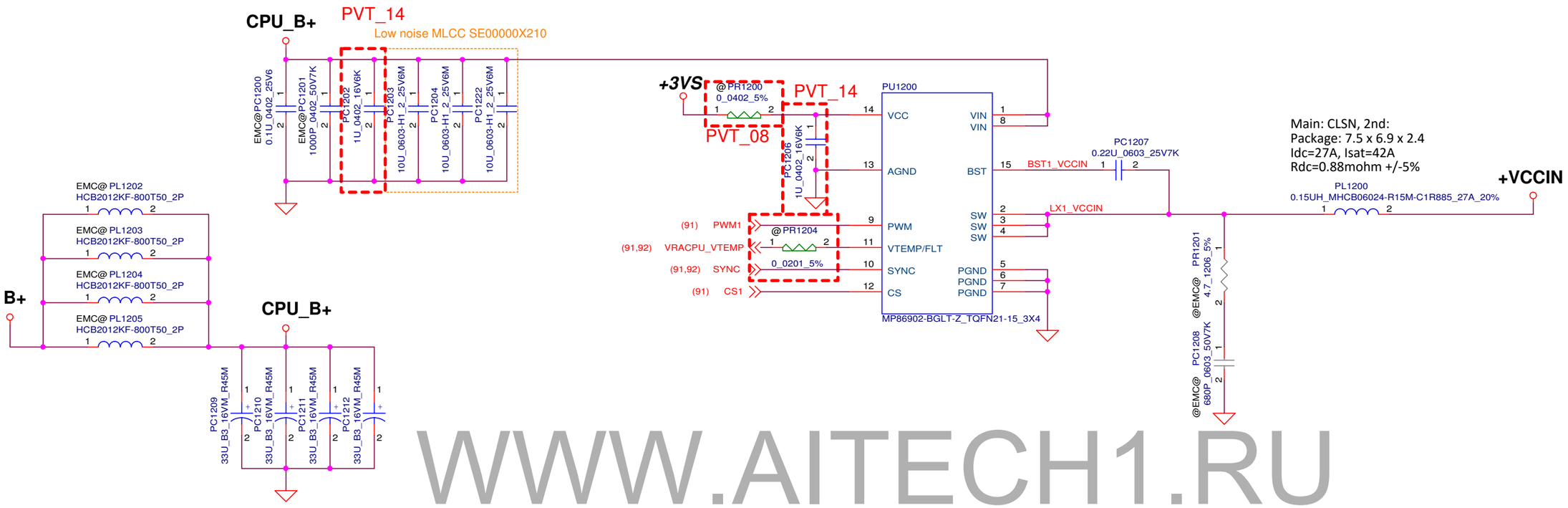

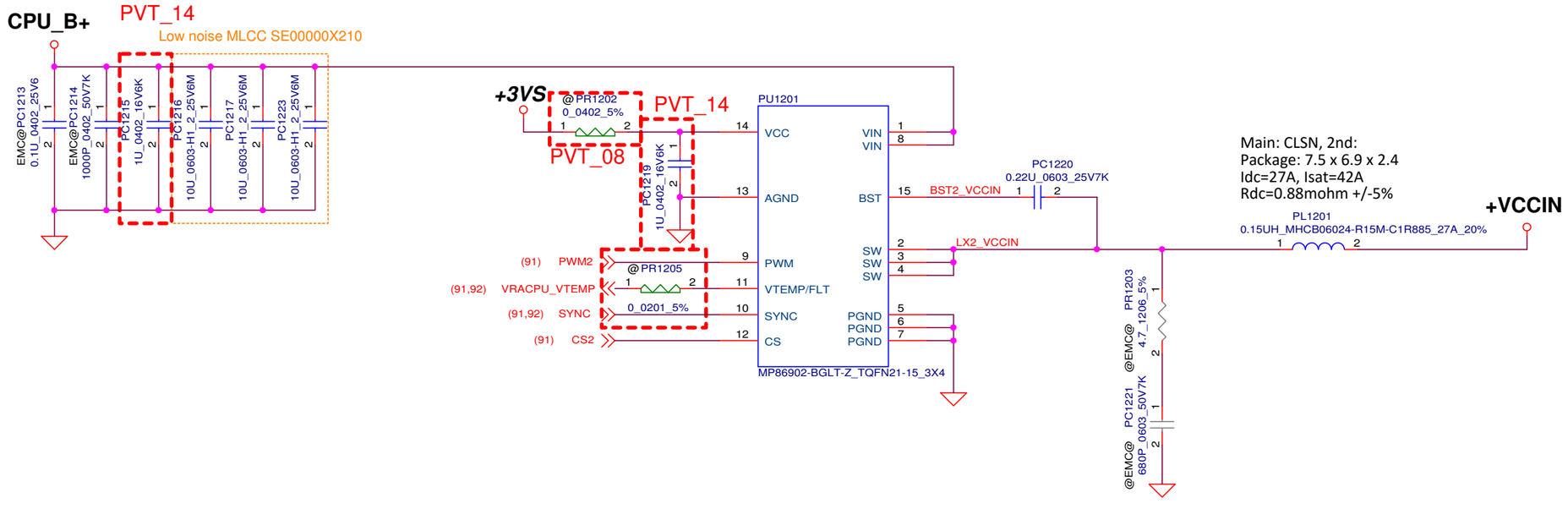

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.			
Title: PWR_VCCIN_Driver MOS			
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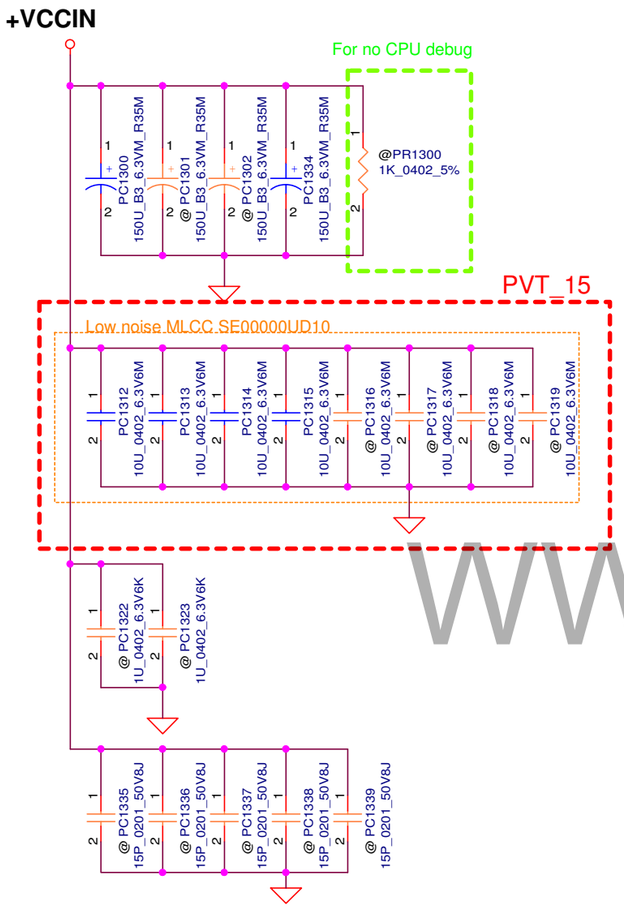
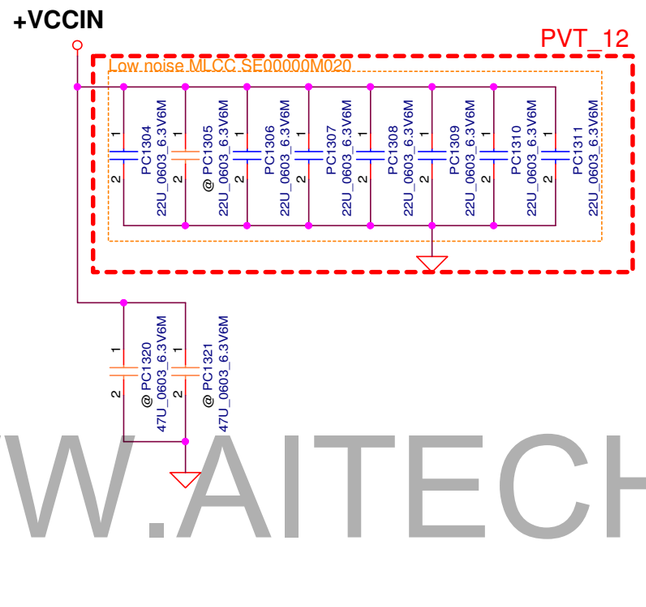
Primary side

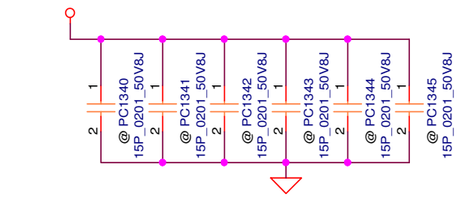


150U_B3 * 4 (pop*2, NC*2)
10U_0402 * 8 (pop*4, NC*4)
22U_0603 * 8 (pop*7, NC*1)
47U_0603 * 2 (NC*2)
1U0402 * 2
1U_0201 * 5 (NC*5)
0.1U_0201 * 5 (NC*5)



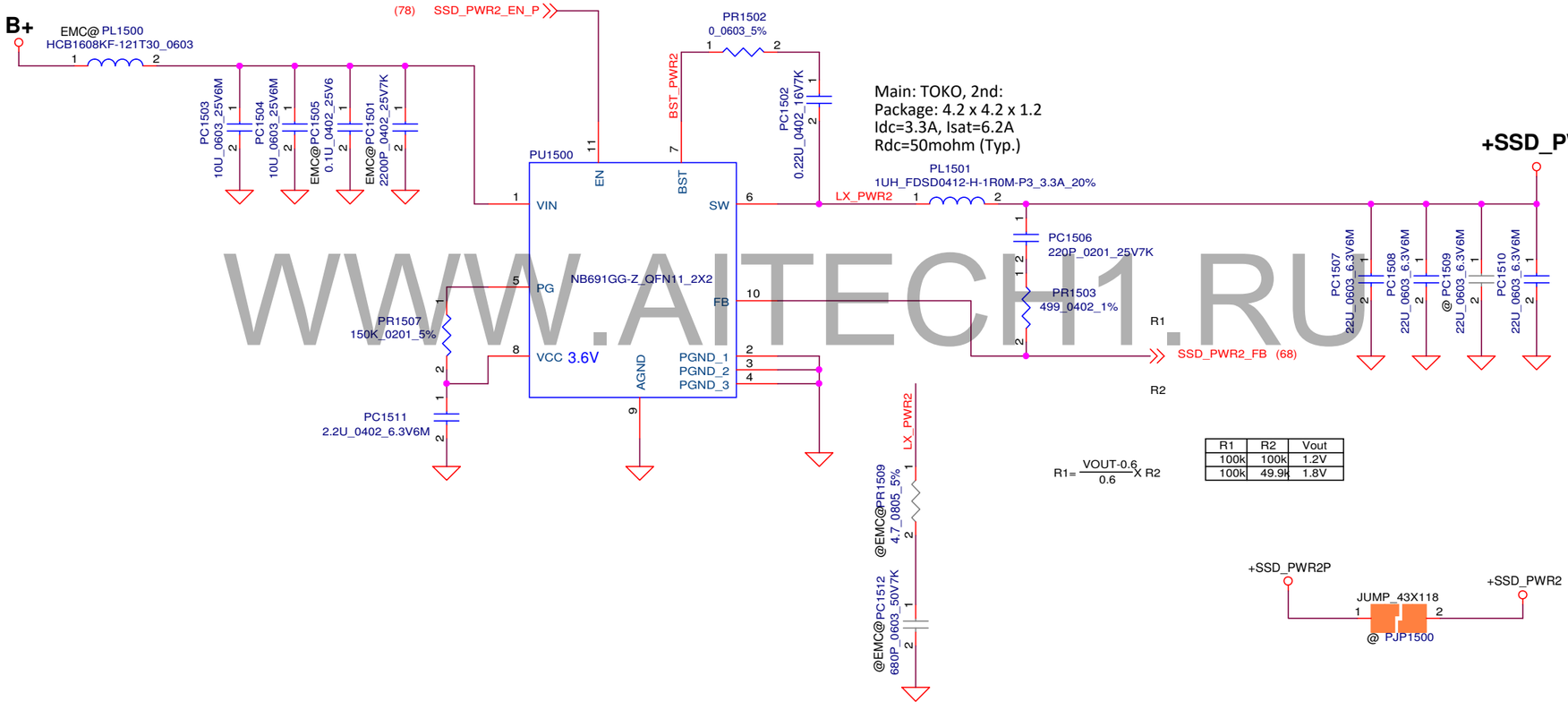
PDG ver 1.35 Primary side:
2x 1uF 0402
4x 10uF 0402
8x 22uF 0603
1x 47uF 0805
2x 330uF 7343

BOT side



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/24	Deciphered Date 2017/08/24	Title PWR_DECOUPLING-VCCIN
			Size Document Number LA-G172P Rev 1.0 (A00)
			Date: Friday, May 24, 2019 Sheet 93 of 101

+1.2VDX_SSD
TDC 1.4A
Peak Current 2A
OCP 7.5A (Typ.)
750kHz



R1	R2	Vout
100k	100k	1.2V
100k	49.9k	1.8V

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: ***PWR_+1.2/+1.8V***

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SSD_PWR3
TDC 1.4A
Peak Current 2A
OCP 8.5A
700kHz

State	CLM	Resistor to GND
M1	8.5A	0
M2	10A	90K
M3	13A	150K
M4	16.5A	>230K or float

PVT_09

@PR1400 0_0201_5%

B+

EMC@ PL1400 HCB2012KF-800T50_2P

@EMC@PC1401 0.1U_0402_25V6

@EMC@PC1402 2200P_0402_50V7K

PC1403 10U_0603_25V6M

PC1404 10U_0603_25V6M

PU1400

NB693GQ-Z_QFN16_3X3

VIN, NC_2, CLM, BST, SW, EN, FB, PG, 3V3, MODE, PGND_1, PGND_2, PGND_3, PGND_4, PGND_5, NC_1

BST_PWR3

PR1401 2.2_0603_5%

PC1400 0.22U_0402_16V7K

LX_PWR3

PL1401 0.68UH_MHCI04015-R68M-R8_5A_20%

Main: CLSN, 2nd:
Package: 4.8 x 4.3 x 1.5
Idc=5A, Isat=8A
Rdc=30mohm (Typ.)

+SSD_PWR3P

PC1405 220P_0201_25V7K

PR1403 499_0402_1%

R1

R2

PC1406 22U_0603_6.3V6M

PC1407 22U_0603_6.3V6M

PC1408 22U_0603_6.3V6M

@ PC1409 22U_0603_6.3V6M

(78) SSD_PWR3_EN_P

SSD_PWR3_FB (68)

PR1406 100K_0201_5%

+3VALW

PR1409 5.1_0402_1%

PC1411 2.2U_0402_6.3V6M

@PR1408 0_0402_5%

PVT_09

R1	R2	Vout
100k	200k	0.9V
100k	120k	1.1V
100k	100k	1.2V

$$R1 = \frac{VOUT-0.6}{0.6} \times R2$$

@EMC@PR1411 4.7_0805_5%

@EMC@PC1412 680P_0603_50V7K

State	VOUT	Fs	Resistor to GND
M1	Vo<3V	700kHz	0
M2	Vo<3V	1000kHz	90K
M3	Vo>=3V	1000kHz	150K
M4	Vo>=3V	700kHz	>230K or float

+SSD_PWR3P

JUMP_43X118

@ PJP1400

+SSD_PWR3

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: ***PWR_+1.2/+1.1/+0.9V***

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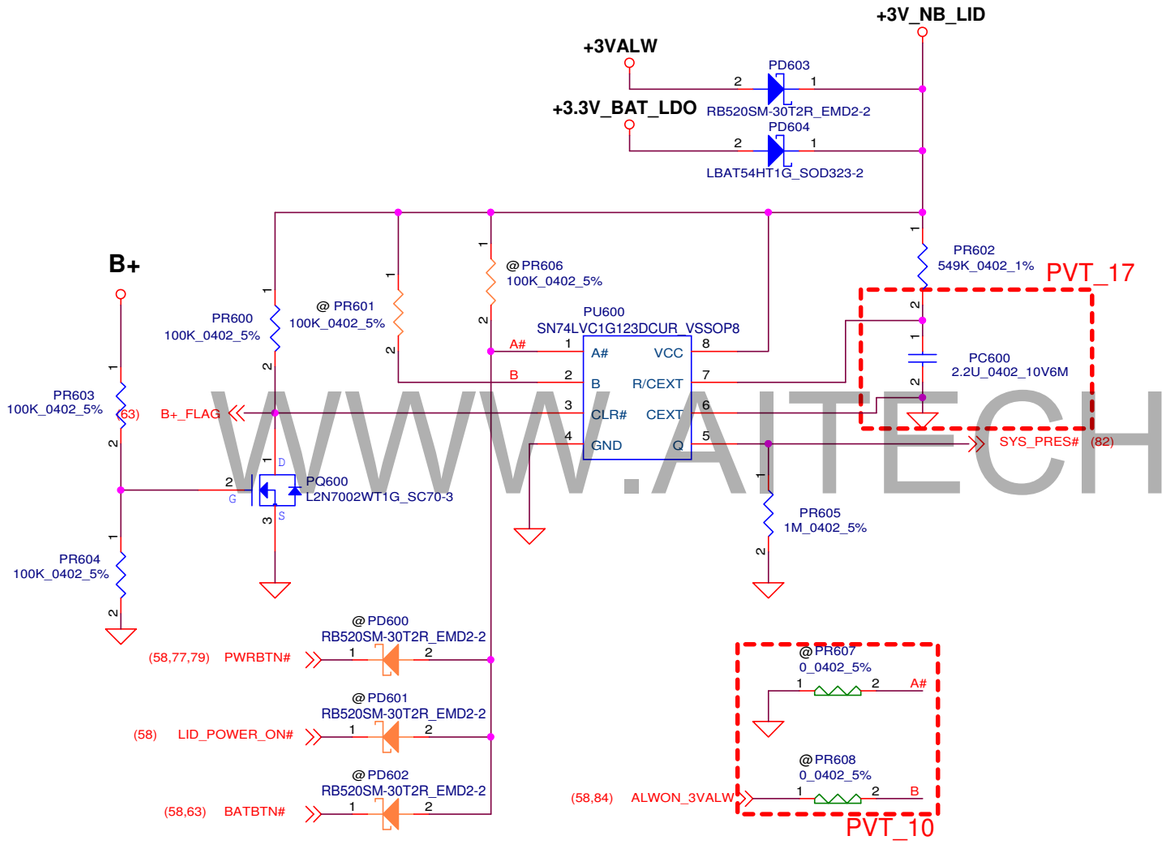

FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⊓
H	↓	H	⊓
↑	L	H	⊓

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.

Title: **PWR_SHIP_MODE**

Size | Document Number: **LA-G172P** | Rev: 1.0 (A00)

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Compal Electronics, Inc.		
Title: ***RESERVE***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 97 of 101	

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.		
Title: ***RESERVE***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 98 of 101	

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.		
Title: ***RESERVE***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
Date: Friday, May 24, 2019	Sheet 99 of 101	

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2017/08/24

Compal Electronics, Inc.		
Title: ***RESERVE***		
Size	Document Number: ***LA-G172P***	Rev: 1.0 (A00)
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CPU Option

UC1 SRG0N@ — SA0000CT62L — ICE LAKE SRG0N

UC1 SRGKL@ — SA0000CT82L — ICE LAKE SRGKL

UC1 SRG0S@ — SA0000CTD2L — ICE LAKE SRG0S

SSD debug Option

R610 TOSHIBA_DB@ — SD043000080 — 0_0201_5%

SSD power Option

Power 3

R6136 NINTEL@ — SD013000080 — 0_0603_5%

LS2 NINTEL@ — SM01000BW00 — HCB1608KF-121T30_0603

TBT Option

URT1 BB@ — SA0000CAH3L — JHL8040R QURW

URT2 BB@ — SA0000CAH3L — JHL8040R QURW

PD Option

UPD1 DJ@ — SA0000CM71L — SN1806026RSHR

UPD2 DJ@ — SA0000CM71L — SN1806026RSHR

WLAN Option

UWL1 KILLER@ — PK29S009L0L — KILLER1650S.01

SSD Option

USSD1 BG4_256GB@ — SA0000C6G1L — KBG40ZPZ256G

USSD1 BG4_512GB@ — SA0000CG61L — KBG40ZPZ512G

USSD1 BG4_1TB@ — SA0000CG21L — KBG40ZPZ1T02

USSD1 INTEL_256GB@ — SA0000C5M2L — SSDPEBKW256G8

USSD1 INTEL_512GB@ — SA0000C7K1L — SSDPEBKW512G8

EC Option

UE1 5105@ — SA00009GL30 — MEC5105_WFBGA169_11X11

UE1 5106@ — SA0000C5D00 — MEC5106_WFBGA169_11X11

CPU I3/I5/I7 Option for different thermal table

I3: RE525 I3@ — SD028240380 — 240K_0402_5%

I5: RE525 I5@ — SD028130380 — 130K_0402_5%

I7: RE525 I7@ — SD028620280 — 62K_0402_5%

EC

CPU I3/I5/I7 Option for different thermal table

I3: RH747 I3@ — SD043100380 — 100K_0201_5%; RH748 I3@ — SD043100380 — 100K_0201_5%

I5: RH747 I5@ — SD043100380 — 100K_0201_5%; RH746 I5@ — SD043100380 — 100K_0201_5%

I7: RH745 I7@ — SD043100380 — 100K_0201_5%; RH748 I7@ — SD043100380 — 100K_0201_5%

BIOS

Pin Name	Micron 8GB SA0000BX51L	Micron 16GB SA0000BX61L	Micron 32GB SA0000BX71L	Hynix 8GB SA0000BYX1L	Hynix 16GB SA0000AW2QL OLD and NO SUPPORT	Hynix 32GB SA0000C7V1L 3733	Samsung 8GB SA0000C6K1L	Samsung 16GB SA0000AU40L OLD and NO SUPPORT	Samsung 32GB SA0000CGN1L	Samsung 16GB SA0000C6L1L NEW	Hynix 16GB SA0000BYW1L NEW	Samsung 4GB SA0000AV71L	Micron 4GB SA0000BWF0L Micron 4GB EOL	Hynix 4GB SA0000AD11L	Hynix 32GB SA0000BWU1L PRTS(4266)
MEM_CONFIG0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
MEM_CONFIG2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1
MEM_CONFIG3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X76 DRAM Option R1

DRAM Config Option (Resistor pop location): MEM_CONFIG4 / MEM_CONFIG3 / MEM_CONFIG2 / MEM_CONFIG1 / MEM_CONFIG0

X7678131L06 — Micron 4GB/3733 (Micron 4GB EOL)

UD1	UD2	UD3	UD4
X76_M4GB_R1@	X76_M4GB_R1@	X76_M4GB_R1@	X76_M4GB_R1@
MT53B256M32D1NP-053 WT	MT53B256M32D1NP-053 WT	MT53B256M32D1NP-053 WT	MT53B256M32D1NP-053 WT
SA0000BWF0L	SA0000BWF0L	SA0000BWF0L	SA0000BWF0L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_M4GB@ RH665 10K_0201_5% SD043100280	X76_M4GB@ RH615 10K_0201_5% SD043100280	X76_M4GB@ RH614 10K_0201_5% SD043100280	X76_M4GB@ RH139 10K_0201_5% SD043100280	X76_M4GB@ RH129 10K_0201_5% SD043100280

X7678131L03 — Micron 8GB/4266

UD1	UD2	UD3	UD4
X76_M8GB_R3@	X76_M8GB_R3@	X76_M8GB_R3@	X76_M8GB_R3@
MT53E512M32D2NP-046 WT	MT53E512M32D2NP-046 WT	MT53E512M32D2NP-046 WT	MT53E512M32D2NP-046 WT
SA0000BX51L	SA0000BX51L	SA0000BX51L	SA0000BX51L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_M8GB@ RH665 10K_0201_5% SD043100280	X76_M8GB@ RH185 10K_0201_5% SD043100280	X76_M8GB@ RH145 10K_0201_5% SD043100280	X76_M8GB@ RH139 10K_0201_5% SD043100280	X76_M8GB@ RH129 10K_0201_5% SD043100280

X7678131L09 — Micron 16GB/4266

UD1	UD2	UD3	UD4
X76_M16GB_R3@	X76_M16GB_R3@	X76_M16GB_R3@	X76_M16GB_R3@
MT53E1G32D4NQ-046 WT	MT53E1G32D4NQ-046 WT	MT53E1G32D4NQ-046 WT	MT53E1G32D4NQ-046 WT
SA0000BX61L	SA0000BX61L	SA0000BX61L	SA0000BX61L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_M16GB@ RH665 10K_0201_5% SD043100280	X76_M16GB@ RH185 10K_0201_5% SD043100280	X76_M16GB@ RH145 10K_0201_5% SD043100280	X76_M16GB@ RH139 10K_0201_5% SD043100280	X76_M16GB@ RH612 10K_0201_5% SD043100280

X7678131L11 — Micron 32GB/4266

UD1	UD2	UD3	UD4
X76_M32GB_R3@	X76_M32GB_R3@	X76_M32GB_R3@	X76_M32GB_R3@
MT53E2G32D8QD-046 WT	MT53E2G32D8QD-046 WT	MT53E2G32D8QD-046 WT	MT53E2G32D8QD-046 WT
SA0000BX71L	SA0000BX71L	SA0000BX71L	SA0000BX71L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_M32GB@ RH665 10K_0201_5% SD043100280	X76_M32GB@ RH185 10K_0201_5% SD043100280	X76_M32GB@ RH145 10K_0201_5% SD043100280	X76_M32GB@ RH613 10K_0201_5% SD043100280	X76_M32GB@ RH129 10K_0201_5% SD043100280

X7678131L07 — Hynix 4GB/3733

UD1	UD2	UD3	UD4
X76_H4GB_R3@	X76_H4GB_R3@	X76_H4GB_R3@	X76_H4GB_R3@
H9HCNNN8KUMLHR-NME	H9HCNNN8KUMLHR-NME	H9HCNNN8KUMLHR-NME	H9HCNNN8KUMLHR-NME
SA0000AD11L	SA0000AD11L	SA0000AD11L	SA0000AD11L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_H4GB@ RH665 10K_0201_5% SD043100280	X76_H4GB@ RH615 10K_0201_5% SD043100280	X76_H4GB@ RH614 10K_0201_5% SD043100280	X76_H4GB@ RH139 10K_0201_5% SD043100280	X76_H4GB@ RH612 10K_0201_5% SD043100280

X7678131L05 — Hynix 8GB/4266

UD1	UD2	UD3	UD4
X76_H8GB_R3@	X76_H8GB_R3@	X76_H8GB_R3@	X76_H8GB_R3@
H9HCNNNBKMALHR-NEE	H9HCNNNBKMALHR-NEE	H9HCNNNBKMALHR-NEE	H9HCNNNBKMALHR-NEE
SA0000BYX1L	SA0000BYX1L	SA0000BYX1L	SA0000BYX1L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_H8GB@ RH665 10K_0201_5% SD043100280	X76_H8GB@ RH185 10K_0201_5% SD043100280	X76_H8GB@ RH145 10K_0201_5% SD043100280	X76_H8GB@ RH613 10K_0201_5% SD043100280	X76_H8GB@ RH612 10K_0201_5% SD043100280

X7678131L12 — Hynix 16GB/4266(NEW)

UD1	UD2	UD3	UD4
X76_H16GB_R3@	X76_H16GB_R3@	X76_H16GB_R3@	X76_H16GB_R3@
H9HCNNNCPMALHR-NEE	H9HCNNNCPMALHR-NEE	H9HCNNNCPMALHR-NEE	H9HCNNNCPMALHR-NEE
SA0000BYW1L	SA0000BYW1L	SA0000BYW1L	SA0000BYW1L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_H16GB@ RH665 10K_0201_5% SD043100280	X76_H16GB@ RH615 10K_0201_5% SD043100280	X76_H16GB@ RH145 10K_0201_5% SD043100280	X76_H16GB@ RH613 10K_0201_5% SD043100280	X76_H16GB@ RH129 10K_0201_5% SD043100280

X7678131L10 — Hynix 32GB/3733

UD1	UD2	UD3	UD4
X76_H32GB_R3@	X76_H32GB_R3@	X76_H32GB_R3@	X76_H32GB_R3@
H9HCNNNFAMALTR-NME	H9HCNNNFAMALTR-NME	H9HCNNNFAMALTR-NME	H9HCNNNFAMALTR-NME
SA0000C7V1L	SA0000C7V1L	SA0000C7V1L	SA0000C7V1L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_H32GB@ RH665 10K_0201_5% SD043100280	X76_H32GB@ RH185 10K_0201_5% SD043100280	X76_H32GB@ RH614 10K_0201_5% SD043100280	X76_H32GB@ RH139 10K_0201_5% SD043100280	X76_H32GB@ RH612 10K_0201_5% SD043100280

X7678131L04 — Samsung 4GB/3733

UD1	UD2	UD3	UD4
X76_S4GB_R3@	X76_S4GB_R3@	X76_S4GB_R3@	X76_S4GB_R3@
K4F8E304HB-MGCJ	K4F8E304HB-MGCJ	K4F8E304HB-MGCJ	K4F8E304HB-MGCJ
SA0000AV71L	SA0000AV71L	SA0000AV71L	SA0000AV71L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_S4GB@ RH665 10K_0201_5% SD043100280	X76_S4GB@ RH615 10K_0201_5% SD043100280	X76_S4GB@ RH145 10K_0201_5% SD043100280	X76_S4GB@ RH613 10K_0201_5% SD043100280	X76_S4GB@ RH612 10K_0201_5% SD043100280

X7678131L08 — Samsung 8GB/4266

UD1	UD2	UD3	UD4
X76_S8GB_R3@	X76_S8GB_R3@	X76_S8GB_R3@	X76_S8GB_R3@
K4U6E3S4AA-MGCL	K4U6E3S4AA-MGCL	K4U6E3S4AA-MGCL	K4U6E3S4AA-MGCL
SA0000C6K1L	SA0000C6K1L	SA0000C6K1L	SA0000C6K1L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_S8GB@ RH665 10K_0201_5% SD043100280	X76_S8GB@ RH185 10K_0201_5% SD043100280	X76_S8GB@ RH614 10K_0201_5% SD043100280	X76_S8GB@ RH613 10K_0201_5% SD043100280	X76_S8GB@ RH129 10K_0201_5% SD043100280

X7678131L13 — Samsung 16GB/4266(NEW)

UD1	UD2	UD3	UD4
X76_S16GB_R3@	X76_S16GB_R3@	X76_S16GB_R3@	X76_S16GB_R3@
K4UBE3D4AA-MGCL	K4UBE3D4AA-MGCL	K4UBE3D4AA-MGCL	K4UBE3D4AA-MGCL
SA0000C6L1L	SA0000C6L1L	SA0000C6L1L	SA0000C6L1L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_S16GB@ RH665 10K_0201_5% SD043100280	X76_S16GB@ RH615 10K_0201_5% SD043100280	X76_S16GB@ RH145 10K_0201_5% SD043100280	X76_S16GB@ RH139 10K_0201_5% SD043100280	X76_S16GB@ RH612 10K_0201_5% SD043100280

X7678131L14 — Samsung 32GB/4266

UD1	UD2	UD3	UD4
X76_S32GB_R3@	X76_S32GB_R3@	X76_S32GB_R3@	X76_S32GB_R3@
K4UCE3Q4AA-MGCL	K4UCE3Q4AA-MGCL	K4UCE3Q4AA-MGCL	K4UCE3Q4AA-MGCL
SA0000CGN1L	SA0000CGN1L	SA0000CGN1L	SA0000CGN1L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_S32GB@ RH665 10K_0201_5% SD043100280	X76_S32GB@ RH615 10K_0201_5% SD043100280	X76_S32GB@ RH145 10K_0201_5% SD043100280	X76_S32GB@ RH139 10K_0201_5% SD043100280	X76_S32GB@ RH129 10K_0201_5% SD043100280

X7678131L21 — Hynix 32GB/4266(PRTS)

UD1	UD2	UD3	UD4
X76_H32GB_R3_P@	X76_H32GB_R3_P@	X76_H32GB_R3_P@	X76_H32GB_R3_P@
H9HCNNNFAMALTR-NEE	H9HCNNNFAMALTR-NEE	H9HCNNNFAMALTR-NEE	H9HCNNNFAMALTR-NEE
SA0000BWU1L	SA0000BWU1L	SA0000BWU1L	SA0000BWU1L

MEM_CONFIG4	MEM_CONFIG3	MEM_CONFIG2	MEM_CONFIG1	MEM_CONFIG0
X76_H32GB_P@ RH665 10K_0201_5% SD043100280	X76_H32GB_P@ RH615 10K_0201_5% SD043100280	X76_H32GB_P@ RH614 10K_0201_5% SD043100280	X76_H32GB_P@ RH613 10K_0201_5% SD043100280	X76_H32GB_P@ RH129 10K_0201_5% SD043100280

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